

## 5 Port 10/100 Ethernet Integrated Switch

*(85nm /Extreme Low Power, PWMT® and AFT® )*

### Features

- 5 port Embedded 10/100 PHY Switch Controller
- IP175G Support 5 100BaseTX
- IP175GH/GHI Support 5 100BaseTX or 4 100Base TX + 1 FX
- Support 1K MAC address entry
- 448K bits packet buffer memory
- 100M PHY support IEEE802.3az at full duplex
- 10M PHY only support 10BaseTe
- Support Auto MDI-MDIX function
- Power Management Tool (PWMT®)
  - APS, auto-power saving while Link-off
  - IEEE 802.3az protocol based power saving
  - WOL+®, light traffic power saving
  - PWD, force-off power saving
- Support Auto Factory Test (AFT®)
- Single Power 3.3V supply
- Built in 1.1V core voltage LDO Regulator
- Two Priority queues per port
- Support 802.1p & DiffServ based QoS
- QoS
  - Port base
  - 802.1p
  - IP DiffServ IPV4/IPV6
  - TCP/UDP port number
  - Pins configure ports priority (VIP port)
- Support max forwarding packet length 1552/1536 bytes option
- Support port mirror function
- Support 1k MAC address
- Support broadcast storm protection
- Support port trunking (LACP)
- Support 16 VLAN (IEEE Std 802.1q)
  - Port-based/Tagged-based VLAN
  - Support insert, remove tag
- Built-in 50 ohm resistors for simplifying BOM
- 85nm Process
- Package and operation temperature
  - IP175G/GH: QFN 48 (6mmx6mm), 0~70℃
  - IP175GHI: QFN 48 (6mmx6mm), -40~85℃

### General Description

- IP175Gx is fabricated with advanced CMOS (85nm) technology and only requires a 3.3V single power supply. This feature makes IP175Gx used very low power consume, such as the full load operation (100Mbps full duplex 5 ports), it only takes 0.45w.
- IP175Gx also supports Power Management Tool (PWMT®) for IEEE 802.3az, APS, WOL+ and PWD for Green Power. While two link devices have no IEEE 802.3az capability, IP175Gx use WOL+ to change link from 100Mbps to 10Mbps for saving power.
- The PWD of IP175Gx is designed for power down switch immediately by pushing a button, user don't plug out the power adapter. Push the button again, it will power on immediately.
- Except Low Power and Rich Power Saving method, IP175Gx supports AFT® for saving Customer Testing Cost. By using a push button and cables, IP175Gx will Auto test completely by itself.
- IP175Gx are available in 48 QFN lead free package.

### Application

- 5 port 10/100 Dumb switch
- 4TX+1FX Dumb Switch

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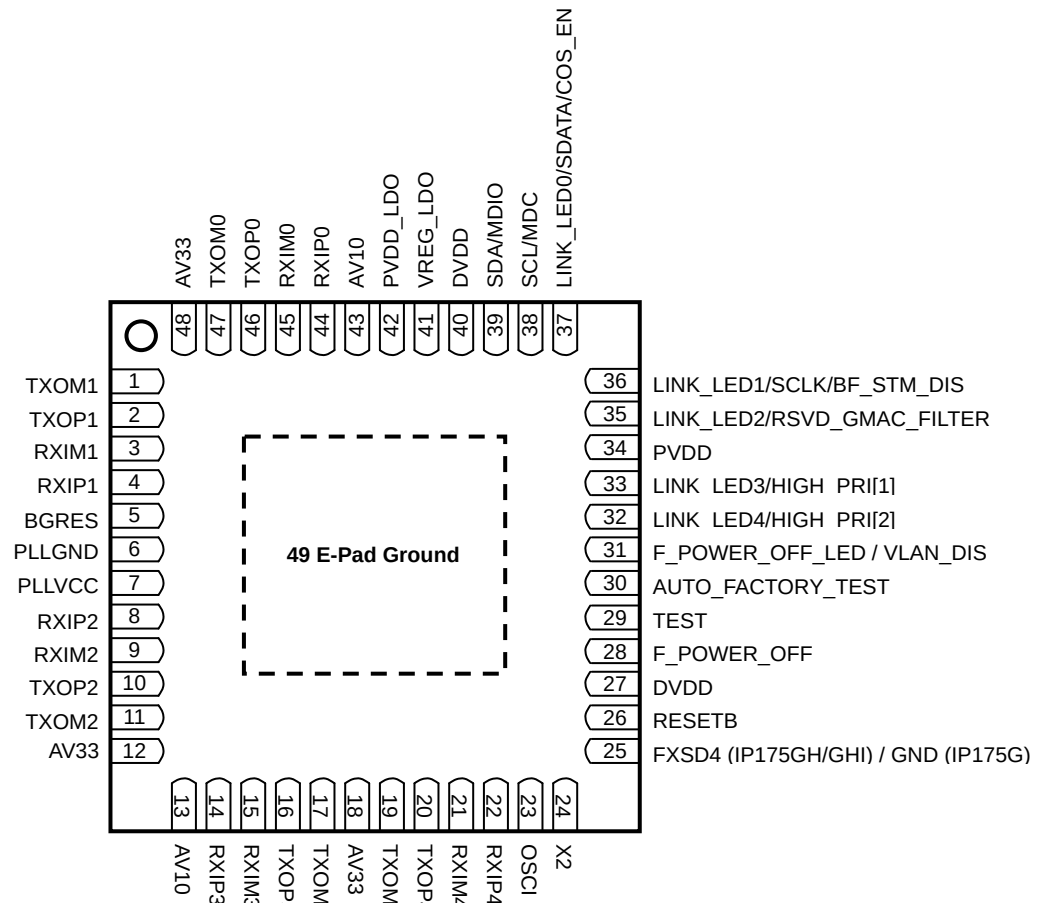
## Revision History

| Revision #     | Date       | Change Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IP175G-DS-R01  | 2012/07/06 | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| IP175Gx-DS-R02 | 2014/06/16 | <ol style="list-style-type: none"><li>1. Add 1.1V power pin description – page 13</li><li>2. Add IP175GH description for fiber application.</li><li>3. Modify 1.1V maxima value to 1.23V – page 62</li><li>4. Add MAC address entry and buffer size description – page 1</li><li>5. Add Serial LED Mode description – page 2</li><li>6. Delete default VLAN Information TPID description – page 60</li><li>7. Remove IP175GI / IP175GHI description</li><li>8. Add LDO parameter description – page 64</li><li>9. Add MDIO output delay Min. parameter description – page 66</li><li>10. Add VIP port description – page 9,12,22</li><li>11. Add PCB footprint – page 76</li><li>12. Add EEPROM interface description – page 23</li><li>13. Delete LED normal operation SPEED and DUPLEX description – page 30</li><li>14. Modify 176 to 175 and 25 to 26 for corrected typing error – page 11,12</li><li>15. Modify page 47 LED_MODE behavior</li><li>16. Swap pin 3,4 and pin 36,37 unumber for corrected typing error – page 11,16</li><li>17. Update pin 31 “F_POWER_OFF_LED” description – page 16</li><li>18. Add Serial LED mode Update Fast description – page 47</li><li>19. Modify Receive/Transmit port to be mirrored description – page 52</li><li>20. Update WOL function enable register from Reg 20 to Reg 22 – page 20</li><li>21. Update WOL function enable Reg 22[15:8] default value from ff to 00– page 64</li></ol> |
| IP175Gx-DS-R03 | 2014/12/03 | <ol style="list-style-type: none"><li>1. Modify PHYx Reg4[15] default value from 1 to 0 for corrected edit error – page 39</li><li>2. Add GHI package description.</li></ol>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## 1 Pin diagram

### 1.1 IP175Gx Pin diagram (QFN48)

(6mm X 6mm Top view)



Exposed pad (pad 49) is system GND, must be soldered to PCB ground plane

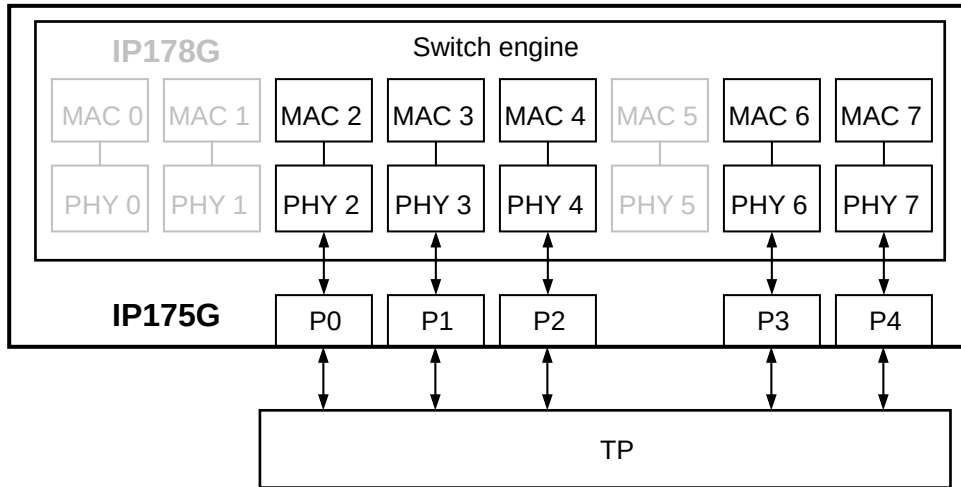
**Figure 1 Pin Diagram**



## 2 IP175Gx application diagram

### 2.1 An 5 TP port switch application

Here shows the application diagram of 5-port switch.



### 2.2 An 5-port switch mixed with a fiber port

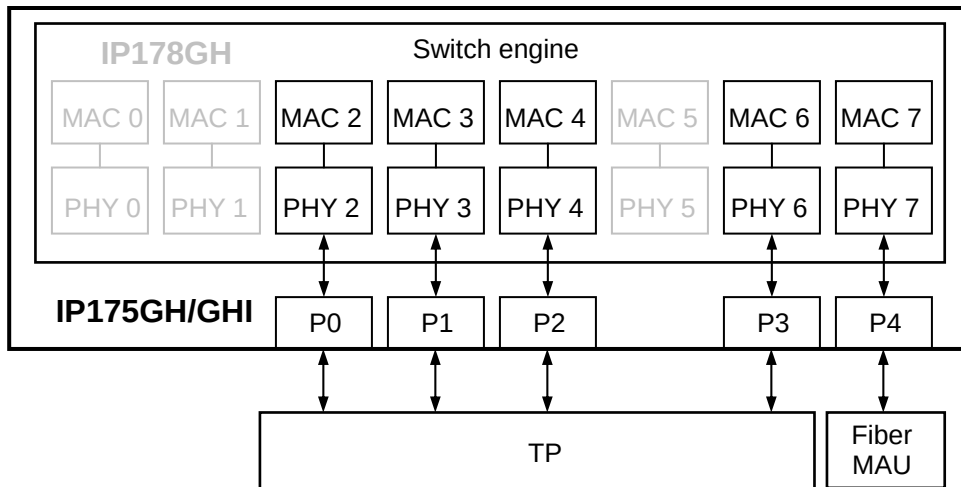
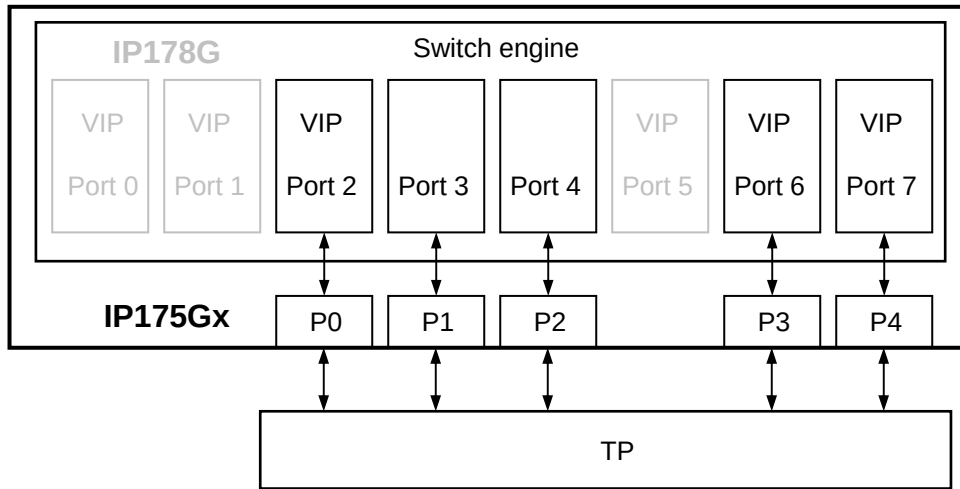


Figure 2 Application Diagram

### 2.3 Switch with VIP ports for specific users from Pin setting



VIP port setting as follow,  
HIGH\_PRI[2:1]

|            |             |             |
|------------|-------------|-------------|
| pin number | 32          | 33          |
| name       | HIGH_PRI[2] | HIGH_PRI[1] |

|                     |                    |
|---------------------|--------------------|
| High priority [2:1] | High priority port |
| 2'b00               | 3,4                |
| 2'b01               | 4                  |
| 2'b1x               | disable            |

### 3 Pin description

Table 1 Pin description

| Type | Description     | Type | Description                                |
|------|-----------------|------|--------------------------------------------|
| I    | Input pin       | IPL  | Input pin with internal pull low 100K ohm  |
| O    | Output pin      | IPH  | Input pin with internal pull high 200K ohm |
| P    | Power or Ground |      |                                            |

#### 3.1 Analog pins

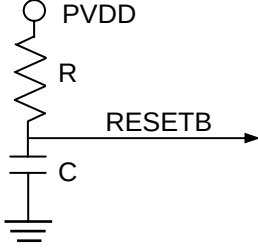
| Pin No.              | Label    | Type | Description                                                              |
|----------------------|----------|------|--------------------------------------------------------------------------|
| <b>LDO Regulator</b> |          |      |                                                                          |
| 41                   | VREG_LDO | P    | LDO regulator output<br>It is an output power pin for 1.1V power source. |
| 42                   | PVDD_LDO | P    | LDO regulator input<br>It is an input power pin for reference voltage.   |

IP175G includes a LDO regulator to convert 3.3V to 1.1V.

#### 3.2 MDI (Media Dependent Interface)

| Pin No.                                          | Label                                                                            | Type | Description                                                                                                                                                                                                                                                                                          |
|--------------------------------------------------|----------------------------------------------------------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Transceiver</b>                               |                                                                                  |      |                                                                                                                                                                                                                                                                                                      |
| 44, 45,<br>4, 3,<br>8, 9,<br>14, 15,<br>22, 21   | RXIP0, RXIM0,<br>RXIP1, RXIM1,<br>RXIP2, RXIM2,<br>RXIP3, RXIM3,<br>RXIP4, RXIM4 | I    | TP receive                                                                                                                                                                                                                                                                                           |
| 46, 47,<br>2, 1,<br>10, 11,<br>16, 17,<br>20, 19 | TXOP0, TXOM0,<br>TXOP1, TXOM1,<br>TXOP2, TXOM2,<br>TXOP3, TXOM3,<br>TXOP4, TXOM4 | O    | TP transmit                                                                                                                                                                                                                                                                                          |
| 25                                               | FXSD4                                                                            | I    | Fiber signal detection of port 4 (IP175GH/GHI)<br>Port 4 can be configured to be either a TP port or a Fiber port with this pin. Connect this pin to GND for TP mode, and do not left this pin floating. Please refer to the paragraph "I/O Electrical Characteristics" for more detail information. |
|                                                  | GND                                                                              | P    | It is GND pin (IP175G.)                                                                                                                                                                                                                                                                              |
| 5                                                | BGRES                                                                            | O    | Band gap resistor.<br>It is connected GND through a precision resistor (R=6.19K, 1%) for band gap reference. Please refer to application circuit for more information.                                                                                                                               |

### 3.3 System clock & reset pins

| Pin No. | Label  | Type | Description                                                                                                                                                                                                                                                                                                    |
|---------|--------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23      | OSCI   | I    | <p>25MHz system clock</p> <p>It is recommended to connect OSCI and X2 to a 25MHz crystal. If the clock source is from another chip or oscillator, the clock should be active at least for 1ms before pin 26 RESETB de-asserted. Pin 24 X2 should be left open in this application.</p>                         |
| 24      | X2     | O    | <p>Crystal pin</p> <p>A 25Mhz crystal can be connected to OSCI and X2.</p>                                                                                                                                                                                                                                     |
| 26      | RESETB | I    | <p>Reset</p> <p>It is a low active input pad with Schmitt trigger. The reset time must be hold for more than 10 ms. If an R/C reset circuit is used, the capacitor should be connected to PVDD as shown in the figure.</p>  |

### 3.4 Boundry scan & test mode

| Pin No. | Label             | Type | Description                                                                       |
|---------|-------------------|------|-----------------------------------------------------------------------------------|
| 29      | TEST              | I    | <p>Test mode enable</p> <p>It should be connected to GND for normal operation</p> |
| 30      | AUTO_FACTORY_TEST | IPL  | Auto Factory Test (AFT®) enable pin                                               |

### 3.5 EEPROM interface /SMI (Serial Management interface)

| Pin No.                                                        | Label    | Type     | Description                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------------|----------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>EEPROM (only 24C02, 24C04, 24C08 &amp; 24C16 supported)</b> |          |          |                                                                                                                                                                                                                                                                                                                                                    |
| 38                                                             | SCL/MDC  | IPL/I    | <p>After reset, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP175Gx stops reading EEPROM if it finds there is no 0x55AA pattern in address 0.</p> <p>After reading EEPROM, this pin will switch to SMI mode MDC input.</p>                                                                                              |
| 39                                                             | SDA/MDIO | IPH, I/O | <p>After reset, it is used as data pin SDA of EEPROM. A bi-directional multi-drop bus for accessing the internal registers. It's recommended to add a 4.7K pull up resistor connecting to PVDD and a 30pf capacitor connecting to ground.</p> <p>After reading EEPROM, this pin will switch to SMI mode MDIO for read/write internal register.</p> |

### 3.6 Frame priority setting

| Pin No.                | Label              | Type        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
|------------------------|--------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----|----|------|-------------|-------------|---------------------|--------------------|-------|-----|-------|---|-------|---------|
| Frame priority setting |                    |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| 33                     | HIGH_PRI[1]        | IPH/O       | <p>Port based priority setting, bit 1</p> <p>It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 3 after reset</p> <p>VIP port setting as follow,<br/>HIGH_PRI[2:1]</p> <table><tr><td>pin number</td><td>32</td><td>33</td></tr><tr><td>name</td><td>HIGH_PRI[2]</td><td>HIGH_PRI[1]</td></tr></table><br><table><tr><td>High priority [2:1]</td><td>High priority port</td></tr><tr><td>2'b00</td><td>3,4</td></tr><tr><td>2'b01</td><td>4</td></tr><tr><td>2'b1x</td><td>disable</td></tr></table> | pin number | 32 | 33 | name | HIGH_PRI[2] | HIGH_PRI[1] | High priority [2:1] | High priority port | 2'b00 | 3,4 | 2'b01 | 4 | 2'b1x | disable |
| pin number             | 32                 | 33          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| name                   | HIGH_PRI[2]        | HIGH_PRI[1] |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| High priority [2:1]    | High priority port |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| 2'b00                  | 3,4                |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| 2'b01                  | 4                  |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| 2'b1x                  | disable            |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |
| 32                     | HIGH_PRI[2]        | IPH/O       | <p>Port based priority setting, bit 2</p> <p>For the port based priority setting, reference HIGH_PRI[1] setting as detail.</p> <p>It is an input signal during reset and its value is latched at the end of reset. This pin acts as a link LED of port 4 after reset</p>                                                                                                                                                                                                                                                                                         |            |    |    |      |             |             |                     |                    |       |     |       |   |       |         |



| Pin No.                | Label  | Type  | Description                                                                                                                                                               |
|------------------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frame priority setting |        |       |                                                                                                                                                                           |
| 37                     | COS_EN | IPH/O | Class of service enable<br><br>Packets with high priority tag are handled as high priority packets if the function is enabled.<br><br>1: disabled (default)<br>0: enable, |

### 3.7 Miscellaneous setting pins

| Pin No.      | Label            | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------|------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Misc.</b> |                  |       |                                                                                                                                                                                                                                                                                                                                                                                                        |
| 28           | F_POWER_OFF      | IPH/I | Force Power Off function for power saving setting pin<br>It should be connected to PVDD for normal operation; pull low 3 seconds to enable Force Power Off function.                                                                                                                                                                                                                                   |
| 31           | VLAN_DIS         | IPH/O | Home VLAN setting enable setting pin.<br>Port 0~Port 3 are all individual VLAN and only send to port 4.<br>1: disable (default)<br>0: enable<br>It is an input signal during reset and its value is latched at the end of reset. This pin acts as a F_POWER_OFF_LED after reset                                                                                                                        |
| 35           | REVD_GMAC_FILTER | IPH/O | Reserved group address filtering<br>It configures how to process the reserved group address, detail see 4.2.                                                                                                                                                                                                                                                                                           |
| 36           | BF_STM_DIS       | IPH/O | Broadcast storm protection enable<br>This function defined in MII register 20.1.[6]<br>1: disable (default)<br>0: enable<br>A port begins to drop incoming packets if it receives broadcast packets more than the threshold defined in MII register 20.9.[15,14]<br>It is an input signal during reset and its value is latched at the end of reset. This pin acts as a link LED of port 1 after reset |

### 3.8 LED interface

| Pin no.                                       | Label                                                         | Type  | Description                                                                                                                                                                           |
|-----------------------------------------------|---------------------------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LED                                           |                                                               |       |                                                                                                                                                                                       |
| 37<br>36<br>35<br>33<br>32                    | LINK_LED0<br>LINK_LED1<br>LINK_LED2<br>LINK_LED3<br>LINK_LED4 | IPH/O | LINK LED<br>It should be connected to PVDD through a LED and resistor.<br>Application circuit<br>   |
| 31                                            | F_POWER_OFF_LED                                               |       | Force Power Off function LED<br><br>It is always low in normal operation and it becomes high if "Force Power Off" function is enabled by pulling low pin 28 for more than 3 seconds.. |
| Serial LED (Enable by MII page 3 register 16) |                                                               |       |                                                                                                                                                                                       |
| 37                                            | SDATA                                                         | IPH/O | LED serial data                                                                                                                                                                       |
| 36                                            | SCLK                                                          | PH/O  | LED serial clock<br>It is a 312.5KHz clock.                                                                                                                                           |

### 3.9 Power & ground pads

| Pad no.  | Label     | Type | Description                                                                                                                                     |
|----------|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 6        | PLL_GND   | P    | Ground of PLL circuit                                                                                                                           |
| 7        | PLL_VCC   | P    | Power of PLL circuit                                                                                                                            |
| 27,40    | DVDD      | P    | <p>Digital Core power</p> <p>These pins must be connect to pin 41 VREG_LDO via a resistor or bead, do not connect to external power supply.</p> |
| 43,13    | AV10      | P    | <p>Analog power</p> <p>These pins must be connect to pin 41 VREG_LDO via a resistor or bead, do not connect to external power supply.</p>       |
| 12,18,48 | AV33      | P    | 3.3V Analog power                                                                                                                               |
| 34       | PVDD      | P    | 3.3V D power                                                                                                                                    |
| 49       | E-pad GND | P    | Exposed pad for system ground, must be soldered to PCB ground plane                                                                             |



## 4 Functional Description

### 4.1 Switch Engine and Queue Management

#### 4.1.1 Switch Engine

IP175Gx integrates an 5-port switch controller, SSRAM, and 5 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE 802.3, IEEE 802.3u, and IEEE 802.3x specifications. IP175Gx offers all the rich features of a high-speed broadband wire Internet services including non-blocking switch fabric

#### 4.1.2 Packet Forwarding

IP175Gx utilizes the “store & forward” method to handle packet transfer. IP175Gx begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

#### 4.1.3 Flow control

IP175Gx jams or pauses a port, which causes output queue over the threshold. Its link partner will defer transmission after detecting the jam or pause frame. A port of IP175Gx defers transmission when it receives a jam or a pause frame. The source address (SA) of pause control frame will be [ IP175Gx OUI (0090C3), port number]. For example, the SA of port 1 pause control frame will be “00 90 C3 00 00 01”.

When CoS is enabled, IP175Gx may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives a high priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

#### 4.1.4 Backpressure

In half duplex mode, the IP175Gx supports backpressure flow control. When set BK\_EN of MII register 20.1[8] to “1”, the packets in buffer reach the threshold, IP175Gx generates a jam pattern to back off the link partner. IP175Gx supports carrier-sense based backpressure. When the carrier-sense based backpressure is enabled, MII register 20.1[7] is set to “0”, and IP175Gx transmits null packets continuously to prevent link partner's transmission when the buffer is not available.

#### 4.1.5 Broadcast storm protection

A port of IP175Gx begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 21.9[15:14] BF\_STM\_THR\_SEL [1:0] in 10ms (100Mbps) or 100ms (10Mbps)

The function can be enabled by pulling low pin 36 BF\_STM\_DIS or programming MII register 20.1[6].

IP175Gx handles multicast frame as a broadcast frame in broadcast storm protection function if MII register 21.30[12] is set to “0”

## 4.2 Rerved Group MAC Address

The table shows the reserved group address for standard use and how frames are processed.

**Table 2 Rerved Group MAC Address table**

| MAC Address           | Protocol                                            | Action                          |                     |
|-----------------------|-----------------------------------------------------|---------------------------------|---------------------|
|                       |                                                     | RSVD_GMAC_FILTER=1<br>(default) | RSVD_GMAC_FILTER =0 |
| 01-80-c2-00-00-00     | Bridge Group Address                                | Forward                         | Forward             |
| 01-80-c2-00-00-01     | MAC Control of IEEE 802.3                           | Drop                            | Drop                |
| 01-80-c2-00-00-02     | Slow protocol address:<br>802.3ad LACP, 802.3ah OAM | Forward                         | Forward             |
| 01-80-c2-00-00-03     | 802.1x                                              | Forward                         | Forward             |
| 01-80-c2-00-00-04     | Reserved for future media<br>access method          | Drop                            | Forward             |
| 01-80-c2-00-00-05     | Reserved for future media<br>access method          | Drop                            | Forward             |
| 01-80-c2-00-00-06     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-07     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-08     | Provider bridge group address                       | Drop                            | Forward             |
| 01-80-c2-00-00-09     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-0A     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-0B     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-0C     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-0D     | Provider bridge GVRP address                        | Drop                            | Forward             |
| 01-80-c2-00-00-0E     | 802.1AB LLDP                                        | Forward                         | Forward             |
| 01-80-c2-00-00-0F     | Reserved for future bridge use                      | Drop                            | Forward             |
| 01-80-c2-00-00-10     | All bridges address                                 | Drop                            | Forward             |
| 01-80-c2-00-00-11to1F | Others                                              | Forward                         | Forward             |
| 01-80-c2-00-00-20     | GMRP                                                | Drop                            | Forward             |
| 01-80-c2-00-00-21     | GVRP                                                | Drop                            | Forward             |
| 01-80-c2-00-00-22to2F | Reserved for future use                             | Drop                            | Forward             |
| 01-80-c2-00-00-30to3F | 802.1ag                                             | Forward                         | Forward             |
| 01-80-c2-00-00-40to4F | Others                                              | Forward                         | Forward             |

### 4.3 Green Power

IP175Gx provides various power management modes to save the power consumption. In addition to the power down mode defined on IEEE802.3, two extra power saving modes are used to further reduce the system power consumption.

#### 4.3.1 Auto Power Saving Mode

IP175Gx will automatically enter this mode if no cable link is established. After entering this mode, IP175Gx will shutdown unnecessary function and issue the link pulse at a rate lower than the regular rate specified on IEEE 802.3.

#### 4.3.2 IEEE802.3az EEE (Energy Efficient Ethernet)

In order to enter this mode, the PHY part should declare the EEE capability during the auto-negotiation phase.

It's the higher layer's responsibility to memorize the link partner's wakeup time and wakeup the link partner before sending data. The higher layer means a mechanism that can evaluate the packet buffer utilization and wake the link partner before sending the data. In general speaking, this mechanism probably consists of at least one of the following items: the packet buffer manager, the application program and OS.

The EEE module works well at LPI (Low Power Idle) mode when

1. Link at full-duplex and
2. Auto-negotiation is enabled in both local and remote PHYs and
3. 100Mbps full duplex and
4. EEE ability is supported in both local & remote PHYs and
5. EEE\_EN (Reg 22.0[7:0]) is enabled for EEE function via default value and
6. SLEEP\_TIMER (Reg 22.1[11:0]) is the default value for EEE sleep timer and
7. WAKE\_TIME (Reg 22.2~9) is the default value for EEE wake time.

#### 4.3.3 WOL+ (Wake On LAN Plus)

IP175Gx not only consumes low power, but also provides various energy-saving methods to save the power. These combined methods make IP175Gx a "green" PHY. The following pictures show the method.

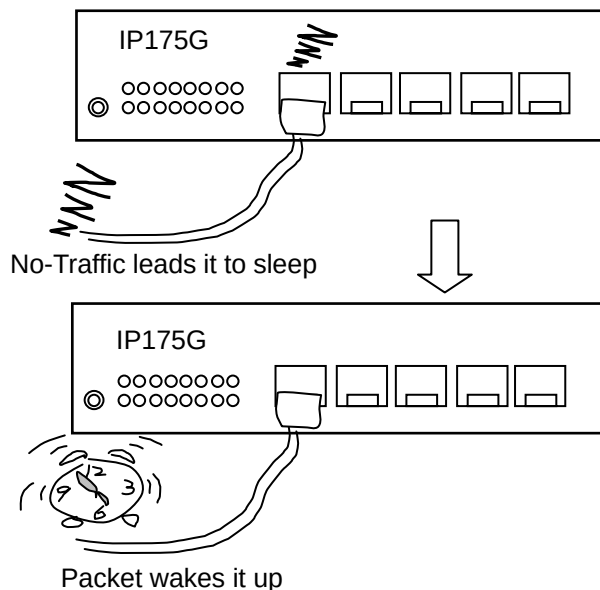


Figure 3 WOL+ Application Diagram

The IP175Gx WOL+ function will be active if a port's RX is in idle state for a period time and this port WOL+ function is enabled (by Reg 22.10[15:8]). This period time can be configured by WOL+ timer register (Reg22.10[1:0]).

This port will be wake up if

- a) Sense magic packet;
- b) Sense link change;
- c) Sense any packet;

The packet format of Magic packet is showing as follows, source address=0x112233445566 for example, repeat this source address 16 times at least.

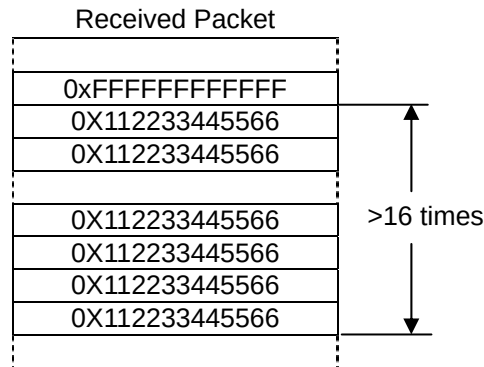


Figure 4 Magic Packet Format

#### 4.3.4 Force Power Off

When "Force power off enable" (pin 28) is pull low for 3 seconds, IP175Gx will enter force power off mode. If "Force power off enable" pin pull low for 3 seconds again, IP175Gx will return normal mode. The expired timer (default value is 3 seconds) is configurable in "FORCE\_POWER\_OFF\_TIME" (MII Register 21.10[7:6]).

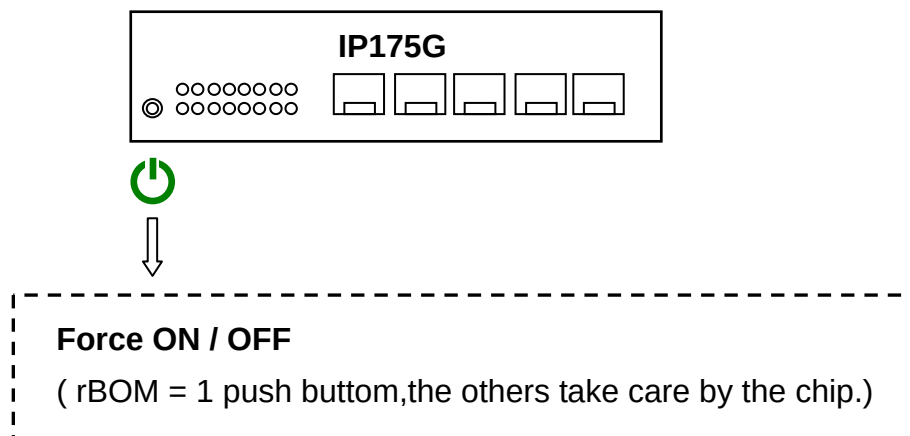


Figure 5 Force Power Off Application Diagram

#### 4.4 Auto Factory Test (AFT) Mode

IP175Gx implements an AFT mechanism, which is very useful for switch pre-test as **Figure 5 AFT system diagrams**. When this function is triggered by hardware pin AFT, IP175Gx physical ports are connected either port-pairs loopback or self-loopback and then IP175Gx will generate frames for TX of all ports and LED will flash.

For example, port1 and port2 are connected to each other (loopback). Check the LED of port1 and port2 is light-on, and then trigger this AFT function and wait a moment trigger again. If the test result is passed (no CRC or packet loss), show LED of port1 and port2 light-on. Otherwise, show LED light-off when CRC or packet loss is happened.

Procedure:

1. Power On
2. Wait for someone Push AFT button to start test
3. IP175Gx transmit packet and LED flash
4. If Push AFT button then goto step 5, else goto step 3
5. LED Show the test result, goto step 2

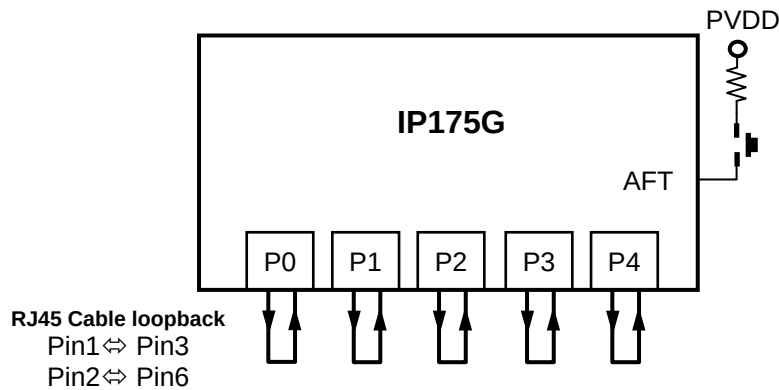


Figure 6 Auto Factory Test Application Diagram

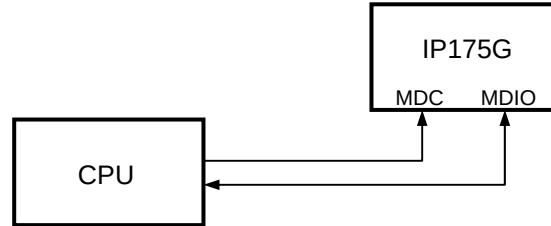
#### 4.5 Reset

**Hardware Reset:** Hardware pin RESETB should be asserted LOW at least for 10ms to reset IP175Gx, and gets initial values from pins, registers and EEPROM after reset.

#### 4.6 Serial management interface

User can access IP175Gx's MII registers through serial management interface with pin MDC and MDIO. Its format is shown in the following table. To access MII register in IP175Gx, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

System diagram



| Frame format    | <Idle><start><op code><PHY address><Registers address><turnaround><data><idle>                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Read Operation  | <Idle><01><10><A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> ><R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub> ><Z0><br><b <sub>15</sub> b <sub>14</sub> b <sub>13</sub> b <sub>12</sub> b <sub>11</sub> b <sub>10</sub> b <sub>9</sub> b <sub>8</sub> b <sub>7</sub> b <sub>6</sub> b <sub>5</sub> b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub> b <sub>0</sub> ><Idle> |
| Write Operation | <Idle><01><01><A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> ><R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub> ><10><br><b <sub>15</sub> b <sub>14</sub> b <sub>13</sub> b <sub>12</sub> b <sub>11</sub> b <sub>10</sub> b <sub>9</sub> b <sub>8</sub> b <sub>7</sub> b <sub>6</sub> b <sub>5</sub> b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub> b <sub>0</sub> ><Idle> |

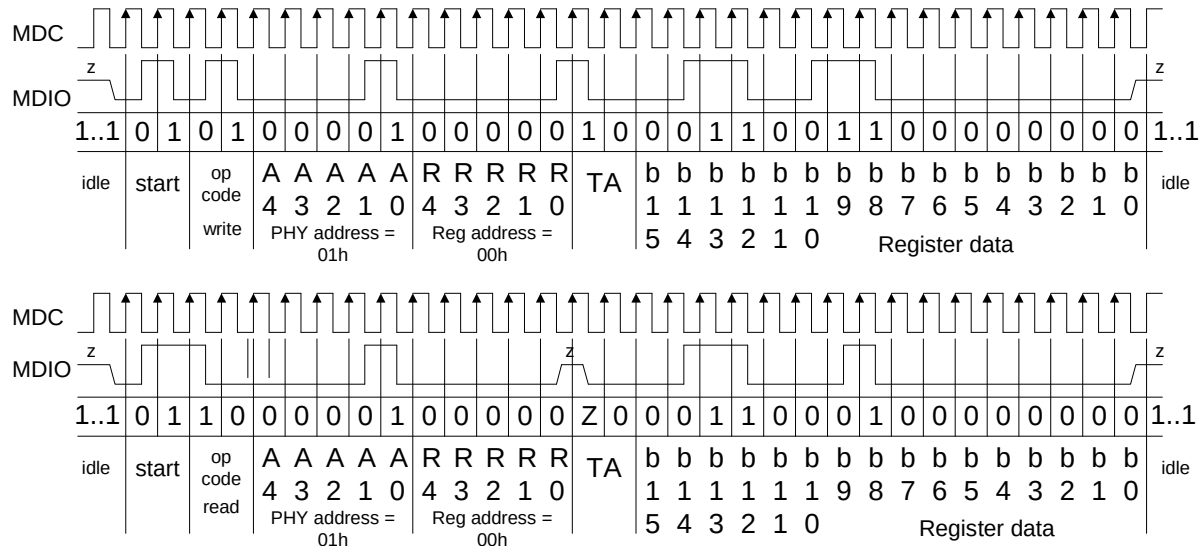


Figure 7 Serial management interface Read / Write Diagram

## 4.7 EEPROM interface

IP175Gx supports EEPROM<sup>1</sup> interface to program configuration registers during power-on reset. When power on and EEPROM is present, if the first 16-bit data match 0x55AA and then the data read from EEPROM until that command-end pattern is read-in.

The EEPROM contents should be configured to three blocks: Command-Start, command and Command-End. Each command contains the full address (PHY address + register address) that you wish to configure as well as 16-bit data, for detail information shown as the following figure.

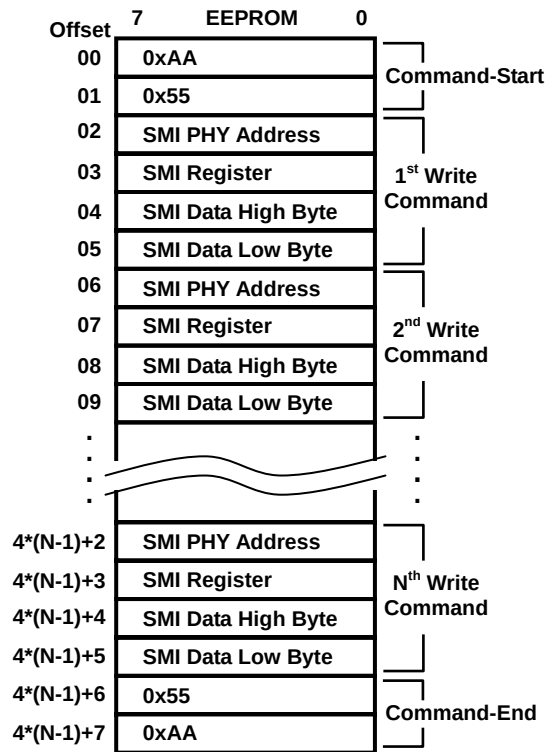


Figure 8 EEPROM data format

<sup>1</sup> Only 24C01, 24C02, 24C04, 24C08 & 24C16 supported.

### 4.7.1 Example: Configure port based VLAN of IP175Gx

Member set: Group A – Port 0, 1, 4  
Group B – Port 2, 3, 4

IP175G Register Setting:

Phy 23.16 = 16'h8c8c  
Phy 23.17 = 16'hffd0  
Phy 23.18 = 16'hdcd0

Serial EEPROM data: AA 55 17 10 8C 8C 17 11 FF D0 17 12 DC D0 55 AA

## 4.8 CoS

IP175Gx supports two types of CoS. One is port base priority function and the other is frame base priority function. IP175Gx supports two levels of priority queues. A high priority packet will be queued to the high priority queue to share more bandwidth. The ratio of bandwidth of high priority and low priority queue is defined in MII register **20.1[15]** or EEPROM **3[7]**.

### 4.8.1 Port base priority

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the corresponding bit in MII register **21.0[9] ~ 21.4[9]** or EEPROM register **65[1] ~ 73[1]**. Each port of IP175Gx can be configured as a high priority port individually.

### 4.8.2 VIP ports

This port based priority function can active either by register or pin setting. There are three pins dedicate for enabling the port based priority function. The follow illustration shows the pin setting part of the port based priority function.

**Table 3 VIP port pin setting table**

|            |             |             |
|------------|-------------|-------------|
| pin number | 32          | 33          |
| name       | HIGH_PRI[2] | HIGH_PRI[1] |

|                     |                    |
|---------------------|--------------------|
| High priority [2:1] | High priority port |
| 2'b00               | 3,4                |
| 2'b01               | 4                  |
| 2'b1x               | disable            |



### 4.8.3 Frame base priority

#### 4.8.3.1 VLAN tag and TCP/IP TOS

IP175Gx examines the specific bits of VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the tag value meets the high priority requirement, that is, VLAN tag or TCP/IP TOS field bigger than 3. It is enabled by programming the corresponding bit in MII register 21.0[10]~21.7[10]. The frame base priority function of each port can be enabled individually.

IP175Gx supports an easy way to enable a sub set of CoS function without programming MII registers. Frame base priority function of all ports is enabled if pin 37 COS\_EN is pulled low. The setting in register takes precedence of the setting on pins.

##### VLAN field

|            |                              |
|------------|------------------------------|
| TYPE= 8100 | TCI(Tag Control Information) |
| Byte 12~13 | 14~15                        |

##### TCI definition

bit [15:13] : User priority 7~0  
bit 12 : Canonical Format Indicator (CFI)  
bit [11:0] : VLAN ID  
IP175Gx uses bit[15:13] to define priority.

##### ToS field

|            |           |
|------------|-----------|
| TYPE= 0800 | IP header |
| Byte 12~13 | 14~15     |

##### IP header definition

##### Byte 14

bit [7:0] : IP protocol version number & header length  
bit [11:0] : VLAN ID  
IP175Gx uses bit[15:13] to define priority.

##### Byte 15 : Service type

bit [7:5] : IP Priority (Precedence) from 7~0  
bit 4 : No Delay (D)  
bit 3 : High Throughput  
bit 2 : High Reliability (R)  
bit [1:0] : Reserved  
IP175Gx uses bit[7:5] to define priority.  
0~3 : Low priority  
4~7 : High priority

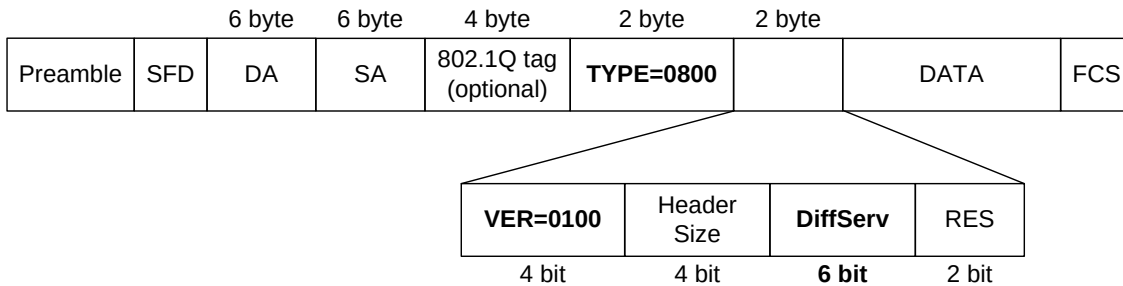
Figure 9 VLAN tag and TCP/IP TOS frame

#### 4.8.3.2 IPv4/IPv6 DiffServ

IP175Gx checks the DiffServ field of a IPv4 frame or Traffic class field [7:2] (TC[7:2]) of a IPv6 frame and uses them to decide the frame's priority if MII register 21.30.[13] DIFFSERV\_EN is enabled. IP175Gx uses DiffServ or TC[7:2] as index to select one of 64 bits. If the bit is "1", the received frame is handled as a high priority frame. IP175Gx recognize the following DSCP (Differentiated Service Code Point) Octet as high priority frame.

6'b101110  
6'b001010  
6'b010010  
6'b011010  
6'b100010  
6'b11x000

##### IPv4 frame format



##### IPv6 frame format

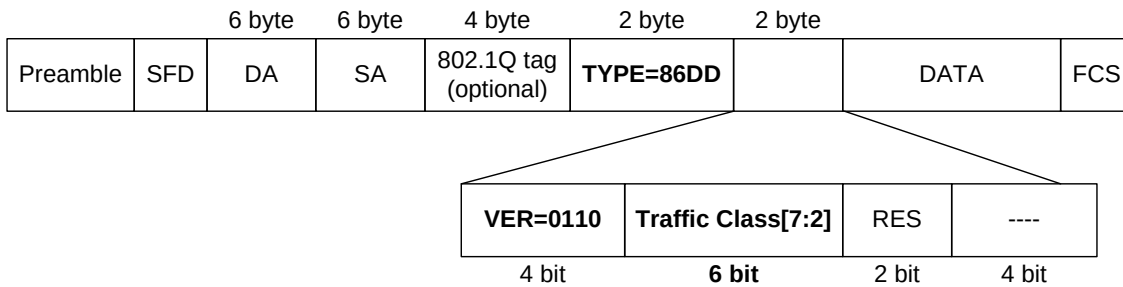


Figure 10 IPv4/IPv6 DiffServ frame

### 4.8.3.3 TCP/UDP logical port priority

IP175Gx can configure the ingress port frame priority by using the TCP/UDP frame logical port number. When the incoming IP packet with TCP or UDP protocols, the 16 bits destination or source port field in the TCP/UDP header can be used for assign the frame priority. It means the source's logical port or the destination's logical port in the incoming packet match any of the pre-defined logical ports, the incoming frame will give a high priority mark and put it in the high priority queue.

TCP/UDP logical port priority function of all ports is enabled if pin 37 COS\_DIS is pulled high. The logical port priority of each pre-defined port number or user defined range of logical port number can be enabled individually by programming the corresponding bit in the MII register 20.14[5:0] or EEPROM register 10[5:0].

**Table 4 TCP/UDP logical port priority table**

#### ■ Pre-defined logical ports list

| Service | TCP  | Description                     |
|---------|------|---------------------------------|
| SSH     | 22   | secure shell                    |
| HTTPs   | 443  | secure HTTP (SSL)               |
| RDP     | 3389 | Windows Remote Desktop Protocol |
| XWIN    | 6000 | X11 – used for X-Windows        |

These pre-defined logical ports can be enable individually by programming MII register 20.14[3:0] or EEPROM register 10[3:0].

#### ■ User defined range logical ports list (defaulting setting)

| Service | TCP  | Description                 |
|---------|------|-----------------------------|
| telnet  | 23   | Remote terminal protocol    |
| VNC     | 5800 | VNC remote desktop protocol |

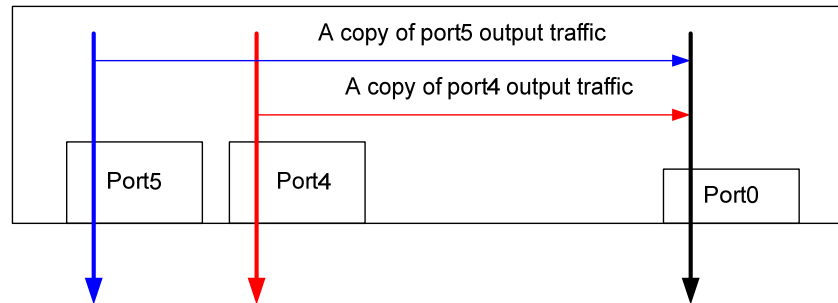
For the user defined range logical ports, it contains two set of range and can be changed by programming via MII register or EEPROM register. Each range consists of a high and low limit register to set the TCP or UDP logical port range. The high limit port number can not large than the low limit port number. The default logical port number of range 0 and 1 are default set to 23 and 5800, for this case the high and low limit port number is the same value. If an incoming IP frame with TCP/UDP port number is between the low and high limit, it will be treated as a high priority frame.

## 4.9 Port Mirroring

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished through assigning 1 to 4 monitored ports and a snooping port. The IP175Gx supports four kinds of monitoring methods: RX(ingress), TX(egress), RX-and-TX, and RX-or-TX. This function can be enabled by programming the corresponding bit in MII registers 20.3 ~ 20.4.

For example, if designer wants to monitor the output traffic of port5 and port4 as shown in the following figure. He has to write "2'b01" to register 20.3[14:13] to choose monitor method to be TX traffic, write 0x30 to registers 20.4[7:0] to select port5 and port4 to be monitored ports, write 1'b1 and 3'b000 to registers 20.3[15] and 20.4[15:13] to select port0 as a monitoring port. IP175Gx will copy tx traffic of port5 and port4 to port0.

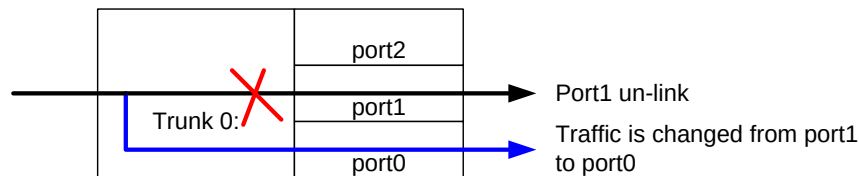


**Figure 11 Port Mirroring Security Block Diagram**

#### 4.10 Link Aggregation

Link aggregation is used to provide a large throughput between two network nodes by using the method of grouping a set of ports. If some of ports are in a trunk group, all ports in that trunk group shall be in the same VLAN group.

Each trunk group may comprise 2 to 4 ports. Designer can configure the trunk group members individually by writing non-zero values to the corresponding bits of a port in the registers 22.12[7:0] and 22.13[7:0] for trunk group 0 and trunk group 1. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP175Gx forwards the packet to the other port of the trunk (auto recovery).



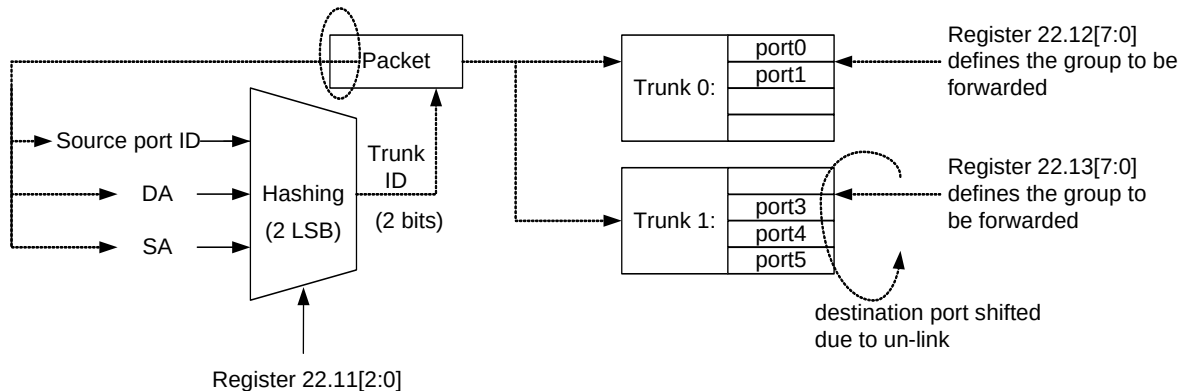
**Figure 12 Trunk Channel Behavior Block Diagram**

To fully utilize the bandwidth in a trunk channel, IP17 5G supports load balance function. A physical port of a trunk forwards a packet only if the trunk group of the packet matches the group setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk group.

The aggregation mode determines which index would be used to search aggregation mask table. Here provide four ways: the four LSB of the SMAC, the four LSB of the DMAC, the four LSB of the SMAC xor DMAC, and Source port ID.

Link aggregation function only uses a 3-bit index to search aggregation mask table. To achieve it, the aggregation index selection is used to extract a 3-bit index from the mentioned in AGGR\_MODE.

If the destination port of a trunk is un-link, the packet will be forward the port shifted by 2. If the port is un-link, too, the packet will be forward the port shifted by 3. For example, if port 3 is un-link, its packet will be forwarded to port 5. If port 5 is un-link, too, the packet will be forwarded to port 4.



**Figure 13 Load Balance Block Diagram**

Link aggregation example:

Here have two trunk groups.

Trunk 0: port 0, 1

Trunk 1: port 5, 6, 7

The link aggregation parameters are set as:

AGGR\_MODE: The aggregation mode determines which index would be used to search aggregation mask table. Here provide four ways:

The four LSB of the SMAC

The four LSB of the DMAC

The four LSB of the SMAC xor DMAC

Source port ID

PHY22 REG11[2:0] = 0x0 (AGGR\_MODE = SMAC)

AGGR\_IDX\_SEL: Link aggregation function only uses a 3-bit index to search aggregation mask table. To achieve it, the aggregation index selection is used to extract 3-bit index from the mentioned in AGGR\_MODE.

PHY22 REG11[4:3] = 0x0 (AGGR\_IDX\_SEL = index[2:0])

AGGR\_GROUP: The port mask is logically grouping a set of ports.

PHY22 REG21[7:0] = 0x03 (AGGR\_GROUP0: port 0 and port 1)

PHY22 REG22[7:0] = 0xe0 (AGGR\_GROUP1: port 5, 6, 7)

Aggregation mask table:

PHY22 REG14[7:0] = 8'b0011\_1101 (AGGR\_MASK0)

PHY22 REG15[7:0] = 8'b0101\_1110 (AGGR\_MASK1)

PHY22 REG16[7:0] = 8'b1001\_1101 (AGGR\_MASK2)

PHY22 REG17[7:0] = 8'b0011\_1110 (AGGR\_MASK3)

PHY22 REG18[7:0] = 8'b0101\_1101 (AGGR\_MASK4)

PHY22 REG19[7:0] = 8'b1001\_1110 (AGGR\_MASK5)

PHY22 REG20[7:0] = 8'b0011\_1101 (AGGR\_MASK6)

PHY22 REG21[7:0] = 8'b0101\_1110 (AGGR\_MASK7)

#### 4.11 Buffer Aging

When buffer aging was enabled, a frame stayed in output port for transmission is discarded if buffer aging time has exceeded one second. The buffer aging time is the maximum delay time for transmission on output port. This function can be set from MII register 20.13.13.

#### 4.12 LED display (normal operation)

| Normal operation                                       |                                                                 |
|--------------------------------------------------------|-----------------------------------------------------------------|
| LED_O_SEL[1:0]                                         | LINK_LED                                                        |
| 00                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX |
| 01                                                     | Off: link fail<br>On: link ok                                   |
| 10                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX |
| 11                                                     | Off: link fail<br>On: link ok<br>Flash: TX/RX                   |
| Flash behavior: Off 105ms → On 105ms → Off 105ms → ... |                                                                 |

#### 4.13 Serial LED Mode

IP175Gx supports serial LED mode and can be setting MII register SERIAL\_LED\_EN to 1 by MII page3 register 16[12].

There are no enough pins for LED and IP175Gx sends out LED information through pin 47 (SCLK) and pin 48 (SDATA). It is necessary to use TTL chip to decode and drive LED. The application circuit is shown below.

IP175Gx supports two types of serial LED mode and can be setting by MII page3 register 16[11]. The default value is 0 (SERIAL\_LED\_MODE = 0) and can be setting to 1 by MII page3 register 16[11].

| Normal operation                                       |                                                                 |                                                         |                                                              |
|--------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------|--------------------------------------------------------------|
| LED_O_SEL[1:0]                                         | LINK_LED                                                        | SPEED_LED                                               | FDX_LED                                                      |
| 00                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: no collision<br>Flash: collision                   | Off: 10 Mbps link fail<br>On: 10 Mbps link ok<br>Flash: TXRX |
| 01                                                     | Off: link fail<br>On: link ok                                   | Off: 10 Mbps<br>On: 100 Mbps                            | Off: half duplex<br>On: full duplex<br>Flash: collision      |
| 10                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex<br>Flash: collision | Off: 10 Mbps link fail<br>On: 10 Mbps link ok<br>Flash: TXRX |
| 11                                                     | Off: link fail<br>On: link ok<br>Flash: TX/RX                   | Off: 10 Mbps<br>On: 100 Mbps                            | Off: half duplex<br>On: full duplex<br>Flash: collision      |
| Flash behavior: Off 105ms → On 105ms → Off 105ms → ... |                                                                 |                                                         |                                                              |

#### 4.13.1 Supports link LED only

IP175Gx supports link LED only when setting SERIAL\_LED\_MODE to 1 and SERIAL\_LED\_EN to 1.

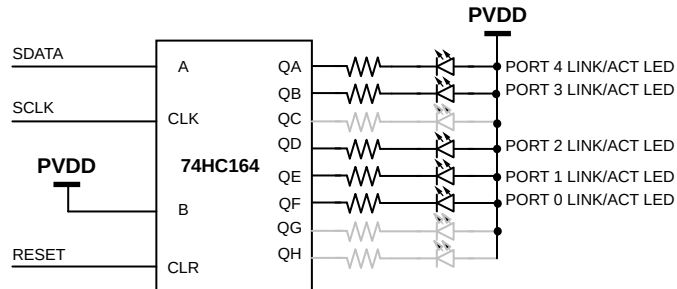


Figure 14 Serial LED Link/Activity Mode

#### 4.13.2 Supports link, speed, and duplex LED

IP175Gx supports link, speed, and duplex LED when setting SERIAL\_LED\_MODE to 0 and SERIAL\_LED\_EN to 1.

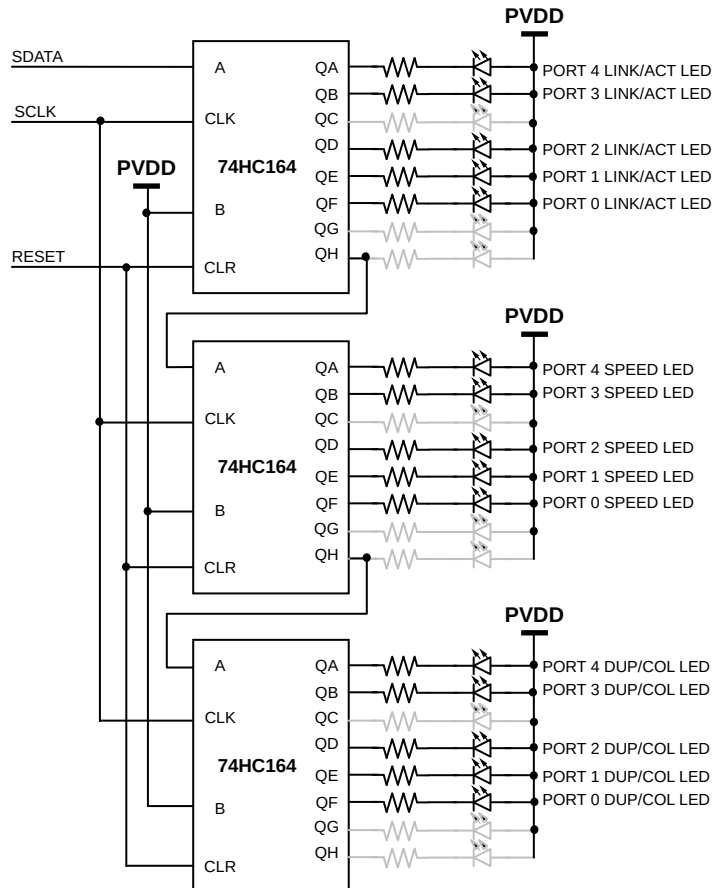


Figure 15 Serial LED Fully Mode

#### 4.14 LED Blink Timing

Table 5 LED Blink Timing

| LED mode                  | Blinking speed                         |
|---------------------------|----------------------------------------|
| Serial mode update period | 10ms                                   |
| Active LED blink          | Off 105ms → On 105ms → Off 105ms → ... |
| Collision LED blink       | Off 105ms → On 105ms → Off 105ms → ... |

#### 4.15 PAD Driving Calibration

This function illustrates the interface between switch and high speed pad groups for pad driving calibration. In default the pad driving capability sets by switch MII register (PHY address 21 Reg10.[14:12]). It also can automatically calibrate to determine pad driving and feedback it to the final pad driving current.

#### 4.16 Fiber port configuration

Port 4 of IP175GH/GHI can be configured to be a fiber port or a TP port individually. A port becomes a fiber port if its FXSDx is connected to a fiber MAU or pulled to high. A port becomes a TP port if it's FXSDx is pulled low.

Table 6 Fiber port Parameter

| PARAMETER                          | SYMBOL    | MIN. | TYP.       | MAX. | UNIT |
|------------------------------------|-----------|------|------------|------|------|
| Fiber Rx common mode Voltage       | $V_{FRC}$ | -    | $AVDD*0.6$ | -    | V    |
| Fiber Rx differential mode Voltage | $V_{FRD}$ | 0.4  | -          | -    | V    |

PVDD = 3.3V

| Voltage on FXSDx | TP port | Fiber port | Fiber signal detect | Condition       |
|------------------|---------|------------|---------------------|-----------------|
| < 0.4 V          | Yes     | --         | --                  |                 |
| > 1.2 V < 1.7 V  | --      | Yes        | Off                 | Fiber unplugged |
| > 1.95 V < 3.3 V | --      | Yes        | On                  | Fiber plugged   |

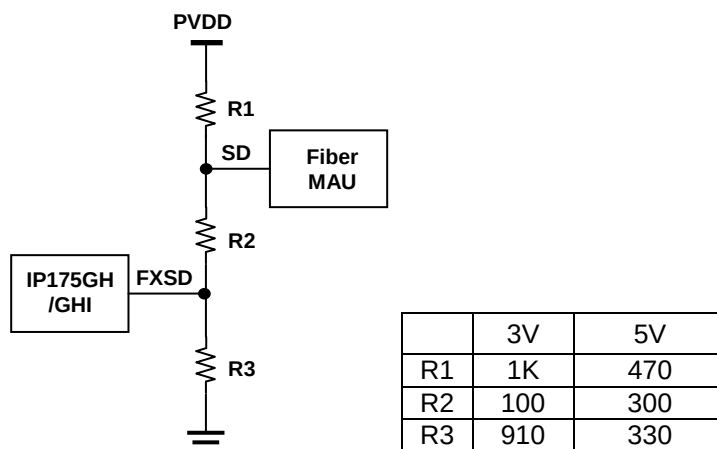


Figure 15 Fiber signal detect application circuit



## 5 Register descriptions

The IP175Gx can be configured via external EEPROM interface at boot time. During operation, IP175Gx registers are accessible via SMI interface.

### 5.1 Register map

#### 5.1.1 MII register map

Table 7 MII register map table

|          | 15                                | 14               | 13                 | 12                 | 11                   | 10                  | 9                        | 8                      | 7                 | 6                   | 5                     | 4                         | 3          | 2               | 1                      | 0                |  |
|----------|-----------------------------------|------------------|--------------------|--------------------|----------------------|---------------------|--------------------------|------------------------|-------------------|---------------------|-----------------------|---------------------------|------------|-----------------|------------------------|------------------|--|
| 20.0     | Software Reset Register ( 55 AA ) |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.1     | priority_rate                     |                  |                    | Reduce_ipg         | drop16               |                     | modify_carrier_algorithm | bk_en                  | bp_kind           | bf_stm_en           |                       |                           | aging      | modbck          | learn_dis_pause        |                  |  |
| 20.2     | tmode_sel                         |                  |                    |                    |                      |                     |                          |                        | input_filter      | hash_mode           |                       |                           |            |                 |                        |                  |  |
| 20.3     | port_mirror_en                    | port_mirror_mode |                    |                    |                      |                     |                          | sel_rx_port_mirror     |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.4     | sel_mirror_port                   |                  |                    | sel_tx_port_mirror |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.5     |                                   |                  |                    |                    |                      |                     |                          |                        |                   | CRC_counter         |                       |                           |            |                 |                        |                  |  |
| 20.6     | pause_trigger                     |                  |                    |                    |                      |                     |                          |                        |                   | pause_flag          |                       |                           |            |                 |                        |                  |  |
| 20.7     | thr_setting                       | read_thr         | wait_backoff       |                    |                      |                     |                          | unit_default_threshold |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.8     | share_high_threshold              |                  |                    |                    |                      |                     |                          |                        |                   | share_low_threshold |                       |                           |            |                 |                        |                  |  |
| 20.9     | pkt_high_threshold                |                  |                    |                    |                      |                     |                          |                        |                   | pkt_low_threshold   |                       |                           |            |                 |                        |                  |  |
| 20.10    | unit_high_threshold               |                  |                    |                    |                      |                     |                          |                        |                   | unit_low_threshold  |                       |                           |            |                 |                        |                  |  |
| 20.11    | mon_en                            |                  |                    |                    |                      |                     |                          | unit_low_num           |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.12    |                                   |                  |                    |                    |                      |                     | share_high_num           |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.13    | fiber_duplex[7:6]                 |                  | buf_aging_en       | src_blk_protect    |                      |                     |                          |                        |                   |                     |                       | port_backpressure_en[7:0] |            |                 |                        |                  |  |
| 20.14    |                                   |                  |                    | lpp_aging_en[4:0]  |                      |                     |                          |                        |                   |                     | userdef_range_en[1:0] | predef_port_en[3:0]       |            |                 |                        |                  |  |
| 20.15    | userdef_range0_high[15:0]         |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.16    | userdef_range0_low[15:0]          |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.17    | userdef_range1_high[15:0]         |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.18    | userdef_range1_low[15:0]          |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 20.19    | fast_mode                         |                  |                    | test_latin         |                      |                     |                          |                        |                   |                     |                       |                           |            |                 | test_sel               |                  |  |
| 21.0     |                                   |                  |                    |                    | port0_cos_en         | port0_high_priority |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.1     |                                   |                  |                    |                    | port1_cos_en         | port1_high_priority |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.2     |                                   |                  |                    |                    | port2_cos_en         | port2_high_priority |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.3     |                                   |                  |                    |                    | port3_cos_en         | port3_high_priority |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.4     |                                   |                  |                    |                    | port4_cos_en         | port4_high_priority |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.5     |                                   |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.6     |                                   |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.7     |                                   |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.8     |                                   |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.9     | bf_stm_thr_sel                    |                  | share_full_thr_sel |                    | unit_default_thr_sel |                     | unit_low_thr_sel         |                        | unit_high_thr_sel |                     |                       |                           | Predrop_en | pkt_low_thr_sel |                        | pkt_high_thr_sel |  |
| 21.10    |                                   | driver[2:0]      |                    |                    | bf_stm_en_qm         | hp_dis_f_low_en     | twopart                  | allpass                | analog_off_time   |                     |                       |                           |            |                 |                        |                  |  |
| 21.11~29 |                                   |                  |                    |                    |                      |                     |                          |                        |                   |                     |                       |                           |            |                 |                        |                  |  |
| 21.30    |                                   |                  | diffserv_en        | bf_fffd_only       | special_add_forward  |                     |                          |                        | fwd_mac_ctl       |                     |                       |                           |            |                 | Drop_extra_long_packet |                  |  |

## 6 PHY registers

**Table 8 PHY Register Map**

| Page | Register | Description                                      | Default | Note          |
|------|----------|--------------------------------------------------|---------|---------------|
| 0    | 0        | Control Register                                 |         | PHY 2,3,4,6,7 |
| 0    | 1        | Status Register                                  |         | PHY 2,3,4,6,7 |
| 0    | 2        | PHY Identifier 1 Register                        |         | SHARE         |
| 0    | 3        | PHY Identifier 2 Register                        |         | SHARE         |
| 0    | 4        | Auto-Negotiation Advertisement Register          |         | PHY 2,3,4,6,7 |
| 0    | 5        | Auto-Negotiation Link Partner Ability Register   |         | PHY 2,3,4,6,7 |
| 0    | 6        | Auto-Negotiation Expansion Register              |         | PHY 2,3,4,6,7 |
| 0    | 7        | Auto-Negotiation Next Page Transmit Register     |         | PHY 2,3,4,6,7 |
| 0    | 8        | Auto-Negotiation Link Partner Next Page Register |         | PHY 2,3,4,6,7 |
| 0    | 13       | MMD Access Control Register                      |         | PHY 2,3,4,6,7 |
| 0    | 14       | MMD Access Address Data Register                 |         | PHY 2,3,4,6,7 |
| 0    | 3.0      | PCS control 1 register                           |         | PHY 2,3,4,6,7 |
| 0    | 3.1      | PCS status 1 register                            |         | PHY 2,3,4,6,7 |
| 0    | 3.20     | EEE capability                                   |         | PHY 2,3,4,6,7 |
| 0    | 3.22     | EEE wake error count                             |         | PHY 2,3,4,6,7 |
| 0    | 7.60     | EEE advertisement register                       |         | PHY 2,3,4,6,7 |
| 0    | 7.61     | EEE link partner ability                         |         | PHY 2,3,4,6,7 |
| 0    | 16       | Special Control Register (APS)                   |         | SHARE         |
| 0    | 18       | Special Status Register                          |         | PHY 2,3,4,6,7 |
| X    | 20       | Page Control Register                            |         | PHY 2,3,4,6,7 |
| 3    | 16       | LED Control Register                             |         | SHARE         |
| 4    | 16       | WOL+ Control Register                            |         | SHARE         |

**Share:** 5 ports share the register

X5: Each port has its individual register

X: indicate do not care.

## Register descriptions

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High

Port 0 PHY address : 2 ;

Port 1 PHY address : 3 ;

Port 2 PHY address : 4 ;

Port 3 PHY address : 6 ;

Port 4 PHY address : 7 ;

### 6.1 MII Register

| PHY                     | MII    | R/W       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  | Default |
|-------------------------|--------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Control Register</b> |        |           |                                                                                                                                                                                                                                                                                                                                                                                                                                              |         |
| 2<br>3<br>4<br>6<br>7   | 0.15   | RW/<br>SC | Reset<br>The PHY is reset if user writes "1" to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP175Gx.                                                                                                                                                                                                                                                                                               | 0       |
|                         | 0.14   | R/W       | Loop back<br>1 = Loop back mode<br>0 = normal operation<br>When this bit set, IP175Gx will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.<br>Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test. | 0       |
|                         | 0.13   | RW        | Speed Selection<br>1 = 100Mbps<br>0 = 10Mbps<br>It is valid only if bit 0.12 is set to be 0.                                                                                                                                                                                                                                                                                                                                                 | 1       |
|                         | 0.12   | RW        | Auto-Negotiation(AN) Enable<br>1 = Auto-Negotiation Enable<br>0 = Auto-Negotiation Disable                                                                                                                                                                                                                                                                                                                                                   | 1       |
|                         | 0.11   | R/W       | Power Down<br>1: power down mode<br>0: normal operation                                                                                                                                                                                                                                                                                                                                                                                      | 0       |
|                         | 0.10   |           | Isolate<br>IP175Gx doesn't support this function.                                                                                                                                                                                                                                                                                                                                                                                            | 0       |
|                         | 0.9    | RW<br>SC  | Restart Auto-Negotiation<br>1 = re-starting Auto-Negotiation<br>0: normal operation                                                                                                                                                                                                                                                                                                                                                          | 0       |
|                         | 0.8    | R/W       | Duplex mode<br>1 = full duplex<br>0 = half duplex<br>It is valid only if bit 0.12 is set to be 0.                                                                                                                                                                                                                                                                                                                                            | 0       |
|                         | 0.7    | R/W       | Collision test                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |
|                         | 0[6:0] | RO        | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0       |

| PHY                    | MII     | R/W      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Default |
|------------------------|---------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Status Register</b> |         |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |         |
| 2<br>3<br>4<br>6<br>7  | 1.15    | RO       | 100Base-T4 capable<br>1 = 100Base-T4 capable<br>0 = not 100Base-T4 capable<br>IP175Gx does not support 100Base-T4. This bit is fixed to be 0.                                                                                                                                                                                                                                                                                                                                                 | 0       |
|                        | 1.14    | RO       | 100Base-X full duplex Capable<br>1 = 100Base-X full duplex capable<br>0 = not 100Base-X full duplex capable                                                                                                                                                                                                                                                                                                                                                                                   | 1       |
|                        | 1.13    | RO       | 100Base-X half duplex Capable<br>1 = 100Base-X half duplex capable<br>0 = not 100Base-X half duplex capable                                                                                                                                                                                                                                                                                                                                                                                   | 1       |
|                        | 1.12    | RO       | 10Base-T full duplex Capable<br>1 = 10Base-T full duplex capable<br>0 = not 10Base-T full duplex capable                                                                                                                                                                                                                                                                                                                                                                                      | 1       |
|                        | 1.11    | RO       | 10Base-T half duplex Capable<br>1 = 10Base-T half duplex capable<br>0 = not 10Base-T half duplex capable                                                                                                                                                                                                                                                                                                                                                                                      | 1       |
|                        | 1[10:7] | RO       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0       |
|                        | 1.6     | RO       | MF preamble Suppression<br>1 = preamble may be suppressed<br>0 = preamble always required                                                                                                                                                                                                                                                                                                                                                                                                     | 1       |
|                        | 1.5     | RO       | Auto-Negotiation Complete<br>1 = Auto-Negotiation complete<br>0 = Auto-Negotiation in progress<br>When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0. | 0       |
|                        | 1.4     | RO<br>LH | Remote fault<br>1 = remote fault detected<br>0 = not remote fault detected<br>When read as logic 1, indicates that IP175Gx has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP175Gx reset.                                                                                                                                                                                 | 0       |
|                        | 1.3     | RO       | Auto-Negotiation Ability<br>1 = Auto-Negotiation capable<br>0 = not Auto-Negotiation capable<br>When read as logic 1, indicates that IP175Gx has the ability to perform Auto-Negotiation.                                                                                                                                                                                                                                                                                                     | 1       |
|                        | 1.2     | RO<br>LL | Link Status<br>1 = Link Pass<br>0 = Link Fail<br>When read as logic 1, indicates that IP175Gx has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.                                                                                                                                                                         | 0       |

| PHY                    | MII | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Default |
|------------------------|-----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Status Register</b> |     |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         |
|                        | 1.1 |     | Jabber Detect<br>1 = jabber condition detected<br>0 = no jabber condition detected<br>When read as logic 1, indicates that IP175Gx has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP175Gx reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled. | 0       |
|                        | 1.0 | RO  | Extended capability<br>1 = Extended register capabilities<br>0 = No extended register capabilities<br>IP175Gx has extended register capabilities.                                                                                                                                                                                                                                                                                                                            | 1       |

| PHY                              | MII | R/W | Description                                                                                                                                                                          | Default  |
|----------------------------------|-----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <b>PHY Identifier 1 Register</b> |     |     |                                                                                                                                                                                      |          |
| 2<br>3<br>4<br>6<br>7            | 2   | RO  | IP175Gx OUI (Organizationally Unique Identifier) ID, the MSB is 3 <sup>rd</sup> bit of IP175Gx OUI ID, and the LSB is 18 <sup>th</sup> bit of IP175Gx OUI ID. IP175Gx OUI is 0090C3. | 16'h0243 |

| PHY                              | MII      | R/W | Description                                                                                                                             | Default |
|----------------------------------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PHY Identifier 2 Register</b> |          |     |                                                                                                                                         |         |
| 2<br>3                           | 3[15:10] | RO  | PHY identifier<br>IP175Gx OUI ID, the MSB is 19 <sup>th</sup> bit of IP175Gx OUI ID, and LSB is 24 <sup>th</sup> bit of IP175Gx OUI ID. | 6'h03   |
| 4<br>6<br>7                      | 3[9:4]   | RO  | Manufacture's Model Number<br>IP175Gx model number                                                                                      | 6'h18   |
|                                  | 3[3:0]   | RO  | Revision Number<br>IP175Gx revision number                                                                                              | 0       |

| PHY                                            | MII    | R/W | Description                                                                                                      | Default  |
|------------------------------------------------|--------|-----|------------------------------------------------------------------------------------------------------------------|----------|
| <b>Auto-Negotiation Advertisement Register</b> |        |     |                                                                                                                  |          |
| 2<br>3<br>4<br>6<br>7                          | 4.15   | R/W | 1 = Next pages are supported<br>0 = Next pages are not supported                                                 | 0        |
|                                                | 4.14   | RO  | Reserved by IEEE, write as 0, ignore on read                                                                     | 0        |
|                                                | 4.13   | R/W | Remote Fault<br>1 = Advertises that this port has detected a remote fault.<br>0 = There is no remote fault.      | 0        |
|                                                | 4.12   | RO  | Reserved for future IEEE use, write as 0, ignore on read                                                         | 0        |
|                                                | 4.11   | RW  | Asymmetric PAUSE<br>1 = Asymmetric flow control is supported<br>0 = Asymmetric flow control is not supported     | 1        |
|                                                | 4.10   | RW  | PAUSE<br>1 = Symmetric flow control is supported<br>0 = Symmetric flow control is not supported                  | 1        |
|                                                | 4.9    | RO  | 100BASE-T4 Not supported                                                                                         | 0        |
|                                                | 4.8    | R/W | 100BASE-TX full duplex<br>1 = 100BASE-TX full duplex is supported<br>0 = 100BASE-TX full duplex is not supported | 1        |
|                                                | 4.7    | R/W | 100BASE-TX<br>1 = 100BASE-TX is supported<br>0 = 100BASE-TX is not supported                                     | 1        |
|                                                | 4.6    | R/W | 10BASE-T full duplex<br>1 = 10BASE-T full duplex is supported<br>0 = 10BASE-T full duplex is not supported       | 1        |
|                                                | 4.5    | R/W | 10BASE-T<br>1 = 10BASE-T is supported<br>0 = 10BASE-T is not supported                                           | 1        |
|                                                | 4[4:0] | RO  | Selector Field<br>Use to identify the type of message being sent by Auto-Negotiation.                            | 5'b00001 |

| PHY                                                   | MII  | R/W | Description                                                                                                                                                                                  | Default |
|-------------------------------------------------------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Auto-Negotiation Link Partner Ability Register</b> |      |     |                                                                                                                                                                                              |         |
| 2<br>3<br>4<br>6<br>7                                 | 5.15 | RO  | Next Page<br>1 = Next Page ability is supported by link partner<br>0 = Next Page ability does not supported by link partner                                                                  | 0       |
|                                                       | 5.14 | RO  | Acknowledge<br>1 = Link partner has received the ability data word<br>0 = Not acknowledge                                                                                                    | 0       |
|                                                       | 5.13 | RO  | Remote Fault<br>1 = Link partner indicates a remote fault<br>0 = No remote fault indicate by link partner<br>If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1. | 0       |
|                                                       | 5.12 | RO  | Reserved by IEEE for future use, write as 0, and read as 0.                                                                                                                                  | 0       |

| PHY | MII    | R/W | Description                                                                                                                                                                                                                                                    | Default  |
|-----|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|     | 5.11   | RO  | Asymmetric PAUSE<br>1 = Link partner support Asymmetric PAUSE<br>0 = Link partner does not support Asymmetric PAUSE<br>When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4.[11:10]. | 0        |
|     | 5.10   | RO  | PAUSE<br>1 = Link partner support Symmetric PAUSE<br>0 = Link partner does not support Symmetric PAUSE<br>When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4.[11:10].              | 0        |
|     | 5.9    | RO  | 100BASE-T4<br>1 = Link partner support 100BASE-T4<br>0 = Link partner does not support 100BASE-T4                                                                                                                                                              | 0        |
|     | 5.8    | RO  | 100BASE-TX full duplex<br>1 = Link partner support 100BASE-TX full duplex<br>0 = Link partner does not support 100BASE-TX full duplex                                                                                                                          | 0        |
|     | 5.7    | RO  | 100BASE-TX<br>1 = Link partner support 100BASE-TX<br>0 = Link partner does not support 100BASE-TX                                                                                                                                                              | 0        |
|     | 5.6    | RO  | 10BASE-T full duplex<br>1 = Link partner support 10BASE-T full duplex<br>0 = Link partner does not support 10BASE-T full duplex                                                                                                                                | 0        |
|     | 5.5    | RO  | 10BASE-T<br>1 = Link partner support 10BASE-T<br>0 = Link partner does not support 10BASE-T<br>When AN is disabled, this bit is set if register 0.13=0                                                                                                         | 0        |
|     | 5[4:0] | RO  | Selector Field<br>Protocol selector of the link partner                                                                                                                                                                                                        | 5'b00000 |

| PHY                                        | MII     | R/W       | Description                                                                                                                                                                                       | Default              |
|--------------------------------------------|---------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| <b>Auto-Negotiation Expansion Register</b> |         |           |                                                                                                                                                                                                   |                      |
|                                            | 6[15:5] | RO        | Reserved                                                                                                                                                                                          | 0                    |
|                                            | 6.4     | RO        | 1 = a fault has been detected via parallel detection function.<br>0 = a fault has not been detected via parallel detection function.                                                              | 0                    |
|                                            | 6.3     | RO        | 1 = Link partner is next page able.<br>0 = Link partner is not next page able.                                                                                                                    | 0                    |
|                                            | 6.2     | RO        | 1 = IP175Gx next page able.<br>0 = IP175Gx is not next page able.                                                                                                                                 | 0                    |
|                                            | 6.1     | RO/<br>LH | 1 = A new page has been received.<br>0 = A new page has not been received.                                                                                                                        | 0                    |
|                                            | 6.0     | RO        | If AN is enabled, this bit means:<br>1 = Link partner is Auto-Negotiation able.<br>0 = Link partner is not Auto-Negotiation able.<br>In 100FX or AN disabled, then this bit is always equal to 0. | 0<br>(AN)<br>(100FX) |

| PHY                                                 | MII     | R/W | Description                                              | Default |
|-----------------------------------------------------|---------|-----|----------------------------------------------------------|---------|
| <b>Auto-Negotiation Next Page Transmit Register</b> |         |     |                                                          |         |
| 2<br>3<br>4<br>6<br>7                               | 7.15    | RW  | Next Page<br>Transmit Code Word Bit 15                   | 0       |
|                                                     | 7.14    | RO  | Reserved<br>Transmit Code Word Bit 14                    | 0       |
|                                                     | 7.13    | RW  | Message Page<br>Transmit Code Word Bit 13                | 1       |
|                                                     | 7.12    | RW  | Acknowledge 2<br>Transmit Code Word Bit 12               | 0       |
|                                                     | 7.11    | RO  | Toggle<br>Transmit Code Word Bit 11                      | 0       |
|                                                     | 7[10:0] | RW  | Message/Unformatted Field<br>Transmit Code Word Bit 10:0 | 1       |

| PHY                                                     | MII     | R/W | Description                                              | Default |
|---------------------------------------------------------|---------|-----|----------------------------------------------------------|---------|
| <b>Auto-Negotiation Link Partner Next Page Register</b> |         |     |                                                          |         |
| 2<br>3<br>4<br>6<br>7                                   | 8.15    | RO  | Next Page<br>Received Code Word Bit 15                   | 0       |
|                                                         | 8.14    | RO  | Acknowledge<br>Received Code Word Bit 14                 | 0       |
|                                                         | 8.13    | RO  | Message Page<br>Received Code Word Bit 13                | 0       |
|                                                         | 8.12    | RO  | Acknowledge 2<br>Received Code Word Bit 12               | 0       |
|                                                         | 8.11    | RO  | Toggle<br>Received Code Word Bit 11                      | 0       |
|                                                         | 8[10:0] | RO  | Message/Unformatted Field<br>Received Code Word Bit 10:0 | 0       |

| PHY                             | MII  | R/W | Description                                                                                                                                                              | Default |
|---------------------------------|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Special Control Register</b> |      |     |                                                                                                                                                                          |         |
| 2<br>3<br>4<br>6<br>7           | 16.7 | RW  | Advance power saving mode<br>1 = Enable APS mode (Default)<br>0 = Disable APS mode<br><br>Please refer to the Power Saving application note for more detail description. | 1       |
|                                 | 16.4 | RW  | Far end fault function<br>1 = Far end fault function disable<br>0 = Far end fault function enable (Default)                                                              | 0       |



| PHY                            | MII   | R/W | Description                                       | Default |
|--------------------------------|-------|-----|---------------------------------------------------|---------|
| <b>Special Status Register</b> |       |     |                                                   |         |
| 2                              | 18.14 | RO  | Linkup<br>1 = linkup<br>0 = unlink                | 0       |
| 3                              | 18.11 | RO  | Speed Mode                                        | 0       |
| 4                              |       |     | 1 = 100 Mbps                                      |         |
| 6                              |       |     | 0 = 10 Mbps                                       |         |
| 7                              | 18.10 | RO  | Duplex Mode<br>1 = Full Duplex<br>0 = Half Duplex | 0       |

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

## 6.2 MMD Control Register

Table 9 MMD Control Register table

| PHY                                | MII       | R/W | Description                                                                                                                                           | Default |
|------------------------------------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>MMD Access Control Register</b> |           |     |                                                                                                                                                       |         |
| 2<br>3<br>4<br>6<br>7              | 13[15:14] | R/W | Function<br>00 = address<br>01 = data, no post increment<br>10 = data, post increment on reads and writes<br>11 = data, post increment on writes only | 0       |
|                                    | 13[13:5]  | R/W | Reserved<br>Write as 0, ignore on read                                                                                                                | 0       |
|                                    | 13[4:0]   | R/W | DEVAD<br>Device Address                                                                                                                               | 0       |

| PHY                                     | MII      | R/W | Description                                                                                                                                                  | Default |
|-----------------------------------------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>MMD Access Address Data Register</b> |          |     |                                                                                                                                                              |         |
| 2<br>3<br>4<br>6<br>7                   | 14[15:0] | R/W | Address Data<br>If 13.15:14 = 00, MMD DEVAD's address register.<br>Otherwise, MMD DEVAD's data register as indicated by the contents of its address register | 0       |

Example 1, Read 2.3.20 (Read Data from MMD register 3.20 of PHY address 2):

1. Write 2.13 = 0x0003 //MMD DEVAD 3
2. Write 2.14 = 0x0014 //MMD Address 20
3. Write 2.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 2.14 //Read MMD Data from 2.3.20

Example 2, Write 3.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 3):

1. Write 3.13 = 0x0007 //MMD DEVAD 7
2. Write 3.14 = 0x003C //MMD Address 60
3. Write 3.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 3.14 = 0x3210 //Write MMD Data 0x3210 to 3.7.60

## 6.3 MMD Data Register

Table 10 MMD Data Register table

| PHY                           | MII        | R/W | Description                                                                                   | Default |
|-------------------------------|------------|-----|-----------------------------------------------------------------------------------------------|---------|
| <b>PCS control 1 Register</b> |            |     |                                                                                               |         |
| 2<br>3<br>4<br>6<br>7         | 3.0[15:11] | RO  | Reserved<br>Ignore when read                                                                  | 0       |
|                               | 3.0.10     | R/W | Clock stop enable<br>1 = IP175Gx may stop xMII Rx clock during LPI<br>0 = Clock not stoppable | 0       |
|                               | 3.0[9:0]   | RO  | Reserved<br>Ignore when read                                                                  | 0       |

| PHY                          | MII        | R/W   | Description                                                                                          | Default |
|------------------------------|------------|-------|------------------------------------------------------------------------------------------------------|---------|
| <b>PCS status 1 Register</b> |            |       |                                                                                                      |         |
| 2<br>3<br>4<br>6<br>7        | 3.1[15:12] | RO    | Reserved<br>Ignore when read                                                                         | 0       |
|                              | 3.1.11     | RO/LH | Tx LPI received<br>1 = Tx PCS has received LPI<br>0 = LPI not received                               | 0       |
|                              | 3.1.10     | RO/LH | Rx LPI received<br>1 = Rx PCS has received LPI<br>0 = LPI not received                               | 0       |
|                              | 3.1.9      | RO    | Tx LPI indication<br>1 = Tx PCS is currently receiving LPI<br>0 = PCS is not currently receiving LPI | 0       |
|                              | 3.1.8      | RO    | Rx LPI indication<br>1 = Rx PCS is currently receiving LPI<br>0 = PCS is not currently receiving LPI | 0       |
|                              | 3.1.7      | RO    | Reserved<br>Ignore on read                                                                           | 0       |
|                              | 3.1.6      | RO    | Clock stop capable<br>1 = The MAC may stop the clock during LPI<br>0 = Clock not stoppable           | 0       |
|                              | 3.1[5:0]   | RO    | Reserved<br>Ignore when read                                                                         | 0       |

| PHY                            | MII        | R/W | Description                                                                                         | Default |
|--------------------------------|------------|-----|-----------------------------------------------------------------------------------------------------|---------|
| <b>EEE capability Register</b> |            |     |                                                                                                     |         |
| 2<br>3<br>4<br>6<br>7          | 3.20[15:7] | RO  | Reserved<br>Ignore when read                                                                        | 0       |
|                                | 3.20.6     | RO  | 10GBASE-KR EEE<br>1 = EEE is supported for 10GBASE-KR<br>0 = EEE is not supported for 10GBASE-KR    | 0       |
|                                | 3.20.5     | RO  | 10GBASE-KX4 EEE<br>1 = EEE is supported for 10GBASE-KX4<br>0 = EEE is not supported for 10GBASE-KX4 | 0       |
|                                | 3.20.4     | RO  | 1000BASE-KX EEE<br>1 = EEE is supported for 1000BASE-KX<br>0 = EEE is not supported for 1000BASE-KX | 0       |
|                                | 3.20.3     | RO  | 10GBASE-T EEE<br>1 = EEE is supported for 10GBASE-T<br>0 = EEE is not supported for 10GBASE-T       | 0       |
|                                | 3.20.2     | RO  | 1000BASE-T EEE<br>1 = EEE is supported for 1000BASE-T<br>0 = EEE is not supported for 1000BASE-T    | 0       |
|                                | 3.20.1     | RO  | 100BASE-TX EEE<br>1 = EEE is supported for 100BASE-TX<br>0 = EEE is not supported for 100BASE-TX    | 1       |
|                                | 3.20.0     | RO  | Reserved<br>Ignore when read                                                                        | 0       |

MMD register 3.22 of Port0~4 (Each PHY has its own MMD register 3.22 with different PHY address)

| PHY                         | MII        | R/W | Description                                                                                                                                                 | Default |
|-----------------------------|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>EEE wake error count</b> |            |     |                                                                                                                                                             |         |
| 2<br>3<br>4<br>6<br>7       | 3.22[15:0] | SC  | EEE wake error count<br>Count wake time faults where IP175Gx fails to complete its normal wake sequence within the time required for the specific PHY type. | 0x0000  |

MMD register 7.60 of Port 0~4 (Each PHY has its own MMD register 7.60 with different PHY address)

| PHY                               | MII        | R/W | Description                                                                                                                              | Default |
|-----------------------------------|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>EEE advertisement Register</b> |            |     |                                                                                                                                          |         |
| 2<br>3<br>4<br>6<br>7             | 7.60[15:7] | RO  | Reserved<br>Ignore when read                                                                                                             | 0       |
|                                   | 7.60.6     | RO  | 10GBASE-KR EEE<br>1 = Advertise that the 10GBASE-KR has EEE capability<br>0 = Do not advertise that the 10GBASE-KR has EEE capability    | 0       |
|                                   | 7.60.5     | RO  | 10GBASE-KX4 EEE<br>1 = Advertise that the 10GBASE-KX4 has EEE capability<br>0 = Do not advertise that the 10GBASE-KX4 has EEE capability | 0       |
|                                   | 7.60.4     | RO  | 1000BASE-KX EEE<br>1 = Advertise that the 1000BASE-KX has EEE capability<br>0 = Do not advertise that the 1000BASE-KX has EEE capability | 0       |
|                                   | 7.60.3     | RO  | 10GBASE-T EEE<br>1 = Advertise that the 10GBASE-T has EEE capability<br>0 = Do not advertise that the 10GBASE-T has EEE capability       | 0       |
|                                   | 7.60.2     | RO  | 1000BASE-T EEE<br>1 = Advertise that the 1000BASE-T has EEE capability<br>0 = Do not advertise that the 1000BASE-T has EEE capability    | 0       |
|                                   | 7.60.1     | R/W | 100BASE-TX EEE<br>1 = Advertise that the 100BASE-TX has EEE capability<br>0 = Do not advertise that the 100BASE-TX has EEE capability    | 1       |
|                                   | 7.60.0     | RO  | Reserved<br>Ignore when read                                                                                                             | 0       |

MMD register 7.61 of Port 0~4 (Each PHY has its own MMD register 7.61 with different PHY address)

| PHY                             | MII        | R/W | Description                                                                                                                                             | Default |
|---------------------------------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>EEE link partner ability</b> |            |     |                                                                                                                                                         |         |
| 2<br>3<br>4<br>6<br>7           | 7.61[15:7] | RO  | Reserved<br>Ignore when read                                                                                                                            | 0       |
|                                 | 7.61.6     | RO  | 10GBASE-KR EEE<br>1 = Link partner is advertising EEE capability for 10GBASE-KR<br>0 = Link partner is not advertising EEE capability for 10GBASE-KR    | 0       |
|                                 | 7.61.5     | RO  | 10GBASE-KX4 EEE<br>1 = Link partner is advertising EEE capability for 10GBASE-KX4<br>0 = Link partner is not advertising EEE capability for 10GBASE-KX4 | 0       |
|                                 | 7.61.4     | RO  | 1000BASE-KX EEE<br>1 = Link partner is advertising EEE capability for 1000BASE-KX<br>0 = Link partner is not advertising EEE capability for 1000BASE-KX | 0       |
|                                 | 7.61.3     | RO  | 10GBASE-T EEE<br>1 = Link partner is advertising EEE capability for 10GBASE-T<br>0 = Link partner is not advertising EEE capability for 10GBASE-T       | 0       |
|                                 | 7.61.2     | RO  | 1000BASE-T EEE<br>1 = Link partner is advertising EEE capability for 1000BASE-T<br>0 = Link partner is not advertising EEE capability for 1000BASE-T    | 0       |
|                                 | 7.61.1     | RO  | 100BASE-TX EEE<br>1 = Link partner is advertising EEE capability for 100BASE-TX<br>0 = Link partner is not advertising EEE capability for 100BASE-TX    | 0       |
|                                 | 7.61.0     | RO  | Reserved<br>Ignore when read                                                                                                                            | 0       |

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

## 6.4 LED mode Control Register

Table 11 LED mode Control Register table

MII page3 register16 of Port 0~4 (5 PHYs share the MII register)

| page                        | MII       | R/W | Description                                                                                                                                                                                     | Default |
|-----------------------------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>LED Control Register</b> |           |     |                                                                                                                                                                                                 |         |
| 3                           | 16[15:14] | R/W | LED_SEL[1:0]<br>LED output mode selection.<br>LED_SEL[1:0]=2'b00: LED mode 0,<br>LED_SEL[1:0]=2'b01: LED mode 1,<br>LED_SEL[1:0]=2'b10: LED mode 2,<br>LED_SEL[1:0]=2'b11: LED mode 3 (default) | 11      |
|                             | 16.12     | RW  | SERIAL_LED_EN<br>1: supports LED serial mode<br>0: supports LED direct mode (default)                                                                                                           | 0       |
|                             | 16.11     | RW  | SERIAL_LED_MODE<br>1: supports link LED only<br>0: supports link, speed, and duplex LED (default)                                                                                               | 0       |
|                             | 16.10     | RW  | SERIAL upd fast<br>1:10ms(default)<br>0:20ms                                                                                                                                                    | 1       |

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

LED mode behavior:

| <b>Normal operation</b>                                |                                                                 |                                                         |                                                              |
|--------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------|--------------------------------------------------------------|
| LED_O_SEL[1:0]                                         | LINK_LED                                                        | SPEED_LED                                               | FDX_LED                                                      |
| 00                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: no collision<br>Flash: collision                   | Off: 10 Mbps link fail<br>On: 10 Mbps link ok<br>Flash: TXRX |
| 01                                                     | Off: link fail<br>On: link ok                                   | Off: 10 Mbps<br>On: 100 Mbps                            | Off: half duplex<br>On: full duplex<br>Flash: collision      |
| 10                                                     | Off: 100 Mbps link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex<br>Flash: collision | Off: 10 Mbps link fail<br>On: 10 Mbps link ok<br>Flash: TXRX |
| 11                                                     | Off: link fail<br>On: link ok<br>Flash: TX/RX                   | Off: 10 Mbps<br>On: 100 Mbps                            | Off: half duplex<br>On: full duplex<br>Flash: collision      |
| Flash behavior: Off 105ms → On 105ms → Off 105ms → ... |                                                                 |                                                         |                                                              |

## 6.5 Register Page mode Control Register

Table 12 Register Page mode Control Register table

MII register 20 of Port 0~4 (Each PHY has its own MII register 20 with different PHY address)

| PHY                          | MII     | R/W | Description            | Default |
|------------------------------|---------|-----|------------------------|---------|
| <b>Page Control Register</b> |         |     |                        |         |
| 2<br>3<br>4<br>6<br>7        | 20[4:0] | RW  | Reg16~31_Page_Sel[4:0] | 00000   |

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

## 6.6 WOL+ Control Register

Table 13 WOL+ Control Register table

| page                             | MII     | R/W | Description                                                                                                                                                                                                                          | Default |
|----------------------------------|---------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PHY WOL+ Control Register</b> |         |     |                                                                                                                                                                                                                                      |         |
| 4                                | 16.[15] | RW  | WOL+ Interrupt Enable<br>Set high to enable WOL+ interrupt<br>1=Enable<br>0=Disable                                                                                                                                                  | 0       |
|                                  | 16.[14] | RW  | WOL+ Level Trigger<br>This bit is used to select the output mode of WOL+ interrupt.<br>1=Level trigger (Low goes high or high goes low when WOL+ interrupt)<br>0=Edge trigger (Positive pulse or negative pulse when WOL+ interrupt) | 1       |
|                                  | 16.[13] | RW  | WOL+ Positive Trigger<br>This bit is used to select the polarity of WOL+ interrupt.<br>1=Low goes high or positive pulse<br>0=High goes low or negative pulse                                                                        | 0       |
|                                  | 16.[12] | RW  | Sense Link Change<br>Set high to enable WOL+ interrupt when link change is sensing.<br>1=Enable<br>0=Disable                                                                                                                         | 1       |
|                                  | 16.[11] | RW  | Sense Magic Packet<br>Set high to enable WOL+ interrupt when magic packet is receiving.<br>1=Enable<br>0=Disable                                                                                                                     | 1       |
|                                  | 16.[10] | RW  | Sense Any Packet<br>Set high to enable WOL+ interrupt when any packet is receiving.<br>1=Enable<br>0=Disable                                                                                                                         | 1       |

| page | MII      | R/W | Description                                                                                                                                                                    | Default |
|------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
|      | 16.[9]   | RW  | Sense DUT<br>Set high to enable WOL+ interrupt when DUT is sensing WOL+ event.<br>1=Enable<br>0=Disable<br>Each PHY address can access the register of the corresponding port. | 1       |
|      | 16.[8]   | RW  | WOL+ Down Speed Enable<br>Set high to enable WOL+ down speed function<br>1=Enable<br>0=Disable                                                                                 | 1       |
|      | 16.[7:1] | RO  | Reserved                                                                                                                                                                       | 0x00    |
|      | 16.[0]   | RO  | PHY WOL+ Interrupt Status<br>The status of PHY WOL+ interrupt is based on the setting of Reg16 Page4 Bit14 and Bit13.                                                          | 1       |

**MII page5 register16 of PHY0 (5 PHYs share the MII register)**

| page                                   | MII      | R/W | Description                                                                                                                          | Default |
|----------------------------------------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PHY WOL+ MAC Address Register 0</b> |          |     |                                                                                                                                      |         |
| 5                                      | 16[15:0] | R/W | WOL+ MAC Address 0 (the most significant word)<br>WOL+ MAC Address = {WOL+_MAC_Address_0,<br>WOL+_MAC_Address_1, WOL+_MAC_Address_2} | 0x0000  |

**MII page6 register16 of PHY0 (5 PHYs share the MII register)**

| page                                   | MII      | R/W | Description                                                                                              | Default |
|----------------------------------------|----------|-----|----------------------------------------------------------------------------------------------------------|---------|
| <b>PHY WOL+ MAC Address Register 1</b> |          |     |                                                                                                          |         |
| 6                                      | 16[15:0] | R/W | WOL+ MAC Address 1<br>WOL+ MAC Address = {WOL+_MAC_Address_0,<br>WOL+_MAC_Address_1, WOL+_MAC_Address_2} | 0x0000  |

**MII page7 register16 of PHY0 (5 PHYs share the MII register)**

| page                                   | MII      | R/W | Description                                                                                                                           | Default |
|----------------------------------------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PHY WOL+ MAC Address Register 2</b> |          |     |                                                                                                                                       |         |
| 7                                      | 16[15:0] | R/W | WOL+ MAC Address 2 (the least significant word)<br>WOL+ MAC Address = {WOL+_MAC_Address_0,<br>WOL+_MAC_Address_1, WOL+_MAC_Address_2} | 0x0000  |

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Example 1, Read page3 register16 (Read Data from page3 register16 of PHY address 2):

1. Write 2.20 = 0x0003 //page3
2. Read 2.16 //Read Data from page3 register16
3. Write 2.20 = 0x0000 //restore to page0

Example 2, Write page3 register16 = 0x3400 (Write Data 0x3400 to page3 register16 of PHY address 2):

1. Write 2.20 = 0x0003 //page3
2. Write 2.16 = 0x3400 //Write Data 0x3400 to page3 register16
3. Write 2.20 = 0x0000 //restore to page0



## 6.7 Switch control registers (I)

Table 14 Switch control registers (I) table

| PHY                                                     | MII     | ROM  | R/W | Description                                                                                                                                                                                                                                                                             | Default |
|---------------------------------------------------------|---------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>EEPROM enable register / Software reset register</b> |         |      |     |                                                                                                                                                                                                                                                                                         |         |
| 20                                                      | --      | 1, 0 |     | EEPROM enable register<br>This register should be filled with 55AA in EEPROM register 0 and 1. IP175Gx will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found. |         |
| 20                                                      | 0       |      | R/W | Software reset register<br>MII register 0 is software reset register. User can reset IP175Gx by writing 55AA to this register.                                                                                                                                                          |         |
| 20                                                      | 0[15]   |      | R   | BFULL_FULL, free buffer is full<br>1: full,<br>0: not full<br>This bit is for debug only.                                                                                                                                                                                               |         |
| 20                                                      | 0[13]   |      | R   | Empty, all output queue is empty<br>1: empty<br>0: not empty<br>This bit is for debug only.                                                                                                                                                                                             |         |
| 20                                                      | 0[12:4] |      |     | Reserved                                                                                                                                                                                                                                                                                |         |
| 20                                                      | 0[3]    |      | R   | PAD_RESET                                                                                                                                                                                                                                                                               |         |
| 20                                                      | 0[2]    |      | R   | EE_RESET1                                                                                                                                                                                                                                                                               |         |
| 20                                                      | 0[1]    |      | R   | SOFT_RESET                                                                                                                                                                                                                                                                              |         |
| 20                                                      | 0[0]    |      | R   | EE_RESET                                                                                                                                                                                                                                                                                |         |
| 20                                                      | 1[15]   |      | R/W | PRIORITY_RATE<br>1: 8 packets<br>0: 16 packets<br><br>Output Queue Scheduling: high priority packet rate                                                                                                                                                                                | 1'b0    |
| 20                                                      | 1[12]   |      | R/W | REDUCE_IPG<br>This function reduce the IPG by random from 0 ~ 20 PPM.<br>1: enable, 0:disable                                                                                                                                                                                           | 1'b1    |
| 20                                                      | 1[11]   |      | R/W | Drop16<br>1: enable, 0:disable                                                                                                                                                                                                                                                          | 1'b0    |
| 20                                                      | 1[9]    |      | R/W | MOD_CARRIER_ALGORITHM<br>Modified carrier based collision algorithm<br>1: enable, 0:disable                                                                                                                                                                                             | 1'b0    |
| 20                                                      | 1[8]    |      | R/W | BK_EN, Backpressure enable<br>1: enable, 0: disable                                                                                                                                                                                                                                     | 1'b1    |
| 20                                                      | 1[7]    |      | R/W | BP_KIND, Backpressure type selection<br>It is valid only if BK_EN is set to 1'b1.<br><br>0: carrier base backpressure<br>1: reserved                                                                                                                                                    | 1'b0    |

| PHY | MII    | ROM  | R/W | Description                                                                                                                                                         | Default |            |         |
|-----|--------|------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------------|---------|
| 20  | 1[6]   |      | R/W | BF_STM_EN, Broadcast storm enable<br>1: enable<br>IP175Gx drops the incoming packet if the number of broadcast packet in queue is over the threshold.<br>0: disable | P(0)    |            |         |
| 20  | 1[3:2] |      | R/W | AGING. Aging time of address table selection<br>An address tag in hashing table will be removed if this function is turned on and its aging timer expires.          | 2'b10   |            |         |
|     |        |      |     |                                                                                                                                                                     |         | Aging time | note    |
|     |        |      |     | 00                                                                                                                                                                  |         | no aging   |         |
|     |        |      |     | 01                                                                                                                                                                  |         | 30s        |         |
|     |        |      |     | 10                                                                                                                                                                  |         | 300s       | default |
|     |        |      |     | 11                                                                                                                                                                  |         | reserved   |         |
| 20  | 1[1]   |      | R/W | MODBCK. Turn on modified back off algorithm<br>The maximum back off period is limited to 8-slot time if this function is turned on.<br>1: turn on, 0: turn off      | 1'b0    |            |         |
| 20  | 1[0]   | 2[0] | R/W | LEARN_DIS_PAUSE<br>0: Enable to learn the SMAC of the received PAUSE frame.<br>1: Disable.                                                                          | 1'b0    |            |         |

## 6.8 Test mode control registers

Table 15 Test mode control registers table

| PHY                                | MII      | R/W | Description                                                                                                                  | Default |
|------------------------------------|----------|-----|------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>Test mode control registers</b> |          |     |                                                                                                                              |         |
| 20                                 | 2[15:10] | R/W | TMODE_SEL. Test mode selection<br>This function is for testing only. The default value must be adopted for normal operation. | 6'h00   |
| 20                                 | 2[8]     |     | Reserved                                                                                                                     |         |
| 20                                 | 2[7]     | R/W | INPUT_FILTER<br>Packet is filtered in input port.<br>1: perform input filtering when queue full<br>0: no operation (default) | 0       |
| 20                                 | 2[6:5]   | R/W | HASH_MODE<br>MAC address table hashing mode<br>00: direct + CRC mapping (default)<br>11: direct mapping                      | 2'b00   |
| 20                                 | 2[4:1]   |     | Reserved                                                                                                                     |         |

## 6.9 Port mirroring control registers

**Table 16 Port mirroring control registers table**

| PHY | MII      | R/W | Description                                                                                                                                                                                 | Default |
|-----|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 20  | 3[15]    | R/W | PORT_MIRROR_EN                                                                                                                                                                              | 1'b0    |
|     | 3[14:13] | R/W | PORT_MIRROR_MODE<br>Select a mirror mode to monitor<br>00: mirror RX (default)<br>01: mirror TX<br>10: mirror RX and TX<br>11: mirror RX or TX                                              | 2'b00   |
|     | 3[12:8]  |     | Reserved                                                                                                                                                                                    |         |
|     | 3[7:0]   | R/W | SEL_RX_PORT_MIRROR<br>Select the source (receive) port to be mirrored<br>0000_0100: port 0 Note 1<br>0000_1000: port 1<br>0001_0000: port 2<br>0100_0000: port 3<br>1000_0000: port 4       | 8'h01   |
|     | 4[15:13] | R/W | SEL_MIRROR_PORT<br>Select a mirror port to monitor any other port<br>010: port 0 Note 1<br>011: port 1<br>100: port 2<br>110: port 3<br>111: port 4 (default)                               | 3'b111  |
|     | 4[12:8]  |     | Reserved                                                                                                                                                                                    |         |
|     | 4[7:0]   | R/W | SEL_TX_PORT_MIRROR<br>Select the destination (transmit) port to be mirrored<br>0000_0100: port 0 Note 1<br>0000_1000: port 1<br>0001_0000: port 2<br>0100_0000: port 3<br>1000_0000: port 4 | 8'h01   |

Note 1 : Port mapping refer Figure 2 Application Diagram

## 6.10 Debug Register

**Table 17 Debug Register table**

| PHY | MII     | R/W      | Description   | Default |
|-----|---------|----------|---------------|---------|
| 20  | 5[15:8] | R/W      | RESERVED      | 16'h0   |
| 20  | 5[7:0]  | RO (SC)  | CRC_COUNTER   | 8'h00   |
| 20  | 6[15:8] | R/W (SC) | PAUSE_TRIGGER | 8'h00   |
| 20  | 6[7:0]  | RO (SC)  | PAUSE_FLAG    | 8'h0    |
| 20  | 7[15]   | R/W      | THR_SETTING   | 1'b0    |

| PHY | MII      | R/W      | Description            | Default |
|-----|----------|----------|------------------------|---------|
| 20  | 7[14]    | R/W (SC) | READ_THR               | 1'b0    |
| 20  | 7[13]    | R/W      | WAIT_BACKOFF           | 1'b0    |
| 20  | 7[12:8]  |          | RESERVED               |         |
| 20  | 7[7:0]   | R/W      | UNIT_DEFAULT_THRESHOLD | 8'd12   |
| 20  | 8[15:8]  | R/W      | SHARE_HIGH_THRESHOLD   |         |
| 20  | 8[7:0]   | R/W      | SHARE_LOW_THRESHOLD    |         |
| 20  | 9[15:8]  | R/W      | PKT_HIGH_THRESHOLD     | 8'd96   |
| 20  | 9[7:0]   | R/W      | PKT_LOW_THRESHOLD      | 8'd80   |
| 20  | 10[15:8] | R/W      | UNIT_HIGH_THRESHOLD    |         |
| 20  | 10[7:0]  | R/W      | UNIT_LOW_THRESHOLD     |         |
| 20  | 11[15]   | R/W      | MON_EN                 | 1'b0    |
| 20  | 11[14:9] |          | RESERVED               |         |
| 20  | 11[8:0]  | RO (SC)  | UNIT_LOW_NUM           | 9'd224  |
| 20  | 12[15:9] |          | RESERVED               |         |
| 20  | 12[8:0]  | RO (SC)  | SHARE_HIGH_NUM         | 9'd224  |

### 6.11 Fiber duplex setting registers

Table 18 Fiber duplex setting registers table

| PHY | MII       | R/W | Description                                                                                                                                                   | Default |
|-----|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 20  | 13[15:14] | R/W | FIBER_DUPLEX<br>Fiber duplex setting for each port.<br>1: fiber port is full-duplex<br>0: fiber port is half_duplex<br>bit[14]: port 4 duplex ability setting | 2'b11   |
| 20  | 13.[13]   | R/W | BUF_AGING_EN                                                                                                                                                  | 1'b0    |
| 20  | 13.[12]   | R/W | SRC_BLK_PROTECT                                                                                                                                               | 1'b1    |
| 20  | 13[11:8]  |     | Reserved                                                                                                                                                      |         |

## 6.12 Backpressure setting registers

| PHY | MII     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Default |
|-----|---------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 20  | 13[7:0] | R/W | <p>PORT_BACKPRESSURE_EN<br/>Backpressure ability setting at half-duplex mode for each port. To ensure this function works correctly, BK_EN (backpressure enable, reg 20.1[8]) should set to logic zero first.</p> <p>1: enable backpressure ability<br/>0: disable</p> <p>bit[7]: port 4 enable backpressure ability    Note 1<br/>bit[6]: port 3 enable backpressure ability<br/>bit[4]: port 2 enable backpressure ability<br/>bit[3]: port 1 enable backpressure ability<br/>bit[2]: port 0 enable backpressure ability</p> | 8'h00   |

## 6.13 TCP/UDP port priority registers

| PHY | MII      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Default  |
|-----|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 20  | 14[15:8] | R/W | <p>LPP_AGING_EN<br/>TCP/UDP logical port priority aging enable<br/>0: disable TCP/UDP logical port priority aging function<br/>1: enable TCP/UDP logical port priority aging function<br/>When this function active, once receive a IP frame with TCP/UDP protocol and the logical port number is the pre-defined port number, the ingress port will treat as a port based high priority port for 300 seconds. After the internal timer expired, the ingress port will change back to previous behavior.</p> <p>bit[15]: port 4 logical port priority aging enable    Note 1<br/>bit[14]: port 3 logical port priority aging enable<br/>bit[12]: port 2 logical port priority aging enable<br/>bit[11]: port 1 logical port priority aging enable<br/>bit[10]: port 0 logical port priority aging enable</p> | 8'h00    |
| 20  | 14[7:6]  |     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |
| 20  | 14[5:4]  | R/W | <p>USERDEF_RANGE_EN<br/>User defined logic port range enable.<br/>bit[1]: user define range 1 register enable<br/>bit[0]: user define range 0 register enable</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 2'b11    |
| 20  | 14[3:0]  | R/W | <p>PREDEF_PORT_EN<br/>Pre-defined logic port number enable.<br/>bit[3]: logic port set 3 enable, port 6000<br/>bit[2]: logic port set 2 enable, port 3389<br/>bit[1]: logic port set 1 enable, port 443<br/>bit[0]: logic port set 0 enable, port 22</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4'hF     |
| 20  | 15       | R/W | <p>USERDEF_RANGE0_HIGH<br/>User defined logic port range 0 high limit</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 16'd23   |
| 20  | 16       | R/W | <p>USERDEF_RANGE0_LOW<br/>User defined logic port range 0 low limit</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 16'd23   |
| 20  | 17       | R/W | <p>USERDEF_RANGE1_HIGH<br/>User defined logic port range 1 high limit</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 16'd5800 |
| 20  | 18       | R/W | <p>USERDEF_RANGE1_LOW<br/>User defined logic port range 1 low limit</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 16'd5800 |

Note 1 : Port mapping refer Figure 2 Application Diagram

#### 6.14 Test mode

| PHY | MII      | R/W | Description                                                                 | Default |
|-----|----------|-----|-----------------------------------------------------------------------------|---------|
| 20  | 19[15]   | R/W | FAST_MODE                                                                   | 1'b0    |
| 20  | 19[11:2] | R/W | TEST_LATIN (only for PHY test mode)                                         | 10'h000 |
| 20  | 19[1:0]  | R/W | TEST_SEL<br>0x0: normal mode<br>0x1: switch test mode<br>0x2: phy test mode | 2'b00   |

#### 6.15 CoS control registers – port 0

| PHY | MII   | R/W | Description                                                                                                                                            | Default |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 2[10] | R/W | Port 0 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 0 are handled as high priority packets. | 1'b0    |
|     | 2[9]  | R/W | Port 0 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 0 are handled as high priority packets.          | 1'b0    |

#### 6.16 CoS control registers – port 1

| PHY | MII   | R/W | Description                                                                                                                                            | Default |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 3[10] | R/W | Port 1 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 1 are handled as high priority packets. | 1'b0    |
|     | 3[9]  | R/W | Port 1 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 1 are handled as high priority packets.          | 1'b0    |

#### 6.17 CoS control registers – port 2

| PHY | MII   | R/W | Description                                                                                                                                            | Default |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 4[10] | R/W | Port 2 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 2 are handled as high priority packets. | 1'b0    |
|     | 4[9]  | R/W | Port 2 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 2 are handled as high priority packets.          | 1'b0    |

### 6.18 CoS control registers – port 3

| PHY | MII   | R/W | Description                                                                                                                                            | Default |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 6[10] | R/W | Port 3 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 3 are handled as high priority packets. | 1'b0    |
|     | 6[9]  | R/W | Port 3 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 3 are handled as high priority packets.          | 1'b0    |

### 6.19 CoS control registers – port 4

| PHY                                      | MII   | R/W | Description                                                                                                                                            | Default |
|------------------------------------------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>CoS and port base VLAN register 4</b> |       |     |                                                                                                                                                        |         |
| 21                                       | 7[10] | R/W | Port 4 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 4 are handled as high priority packets. | 1'b0    |
|                                          | 7[9]  | R/W | Port 4 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 4 are handled as high priority packets.          | 1'b0    |

### 6.20 Switch control registers (IV)

| PHY | MII      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                    | Default |
|-----|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 9[15:14] | R/W | BF_STM_THR_SEL[1:0].<br>Broadcast storm threshold selection<br>00: 2 packets/10ms for 100Mbps port, or 2 packets/100ms for 10Mbps port,<br>01: 6 packets/10ms for 100Mbps port, or 6 packets/100ms for 10Mbps port,<br>10: 14 packets/10ms for 100Mbps port, or 14 packets/100ms for 10Mbps port,<br>11: 30 packets/10ms for 100Mbps port, or 30 packets/100ms for 10Mbps port | 2'b00   |
|     | 9[13:12] | R/W | SHARE_FULL_THR_SEL[1:0].<br>Share buffer threshold selection<br>00: 160 units<br>01: 180 units<br>10: 140 units<br>11: 120 units                                                                                                                                                                                                                                               | 2'b00   |
|     | 9[11:10] | R/W | UNIT_DEFAULT_THR_SEL[1:0].<br>Output Queue minimum threshold selection<br>00: 40 units<br>01: 32 units<br>10: 48 units<br>11: 56 units                                                                                                                                                                                                                                         | 2'b00   |

| PHY | MII       | R/W | Description                                                                                                                                                                                                                                                                           | Default    |
|-----|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
|     | 9[9:8]    | R/W | UNIT_LOW_THR_SEL                                                                                                                                                                                                                                                                      | 2'b00      |
|     | 9[7:6]    | R/W | UNIT_HIGH_THR_SEL[1:0].<br>Output Queue Flow control ON threshold selection<br>If share buffer is over share buffer full threshold, Output Queue Flow control ON threshold will be dynamic changed to 28.<br>Others,<br>00: 50 units<br>01: 70 units<br>10: 90 units<br>11: 110 units | 2'b00      |
|     | 9[5]      |     | Reserved                                                                                                                                                                                                                                                                              |            |
|     | 9[4]      | R/W | PREDROP_EN<br>1: Drop an incoming broadcast packet if any port is congested.<br>0: forward an incoming broadcast packet to un-congested ports instead of congested ports.                                                                                                             | 1'b0       |
|     | 9[3:2]    | R/W | PKT_LOW_THR_SEL[1:0].<br>Packet low water mark threshold selection<br>00: 40 units<br>01: 30 units<br>10: 20 units<br>11: 10 units                                                                                                                                                    | 2'b00      |
|     | 9[1:0]    | R/W | PKT_HIGH_THR_SEL[1:0].<br>Packet high water mark threshold selection<br>00: 50 units<br>01: 40 units<br>10: 30 units<br>11: 20 units                                                                                                                                                  | 2'b00      |
| 21  | 10[15]    |     | RESERVED                                                                                                                                                                                                                                                                              |            |
| 21  | 10[14:12] | R/W | DRIVER[2:0]<br>Pad Drive Current<br>000: 0 mA<br>001: 1.5 mA<br>010: 4.6 mA (default)<br>011: 9.9 mA<br>100: 9.9 mA<br>101: 9.9 mA<br>110: 15.1 mA<br>111: 18.4 mA                                                                                                                    | 3'b<br>010 |
| 21  | 10[11]    | R/W | BF_STM_EN_QM                                                                                                                                                                                                                                                                          | 1'b0       |
| 21  | 10[10]    | R/W | HP_DIS_FLOW_EN<br>Disable flow control when recived high priority packet                                                                                                                                                                                                              | 1'b0       |
| 21  | 10[9]     | R/W | TWOPART                                                                                                                                                                                                                                                                               | 1'b1       |
| 21  | 10[8]     | R/W | ALLPASS<br>All packet forwarded include CRC packet.                                                                                                                                                                                                                                   | 1'b0       |



| PHY | MII     | R/W | Description                                                                                                                                                                                    | Default |
|-----|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 10[7:6] | R/W | ANALOG_OFF_TIME<br>The length of time of the push button input must be held low in order to turn off analog power<br><br>0x0: 1.5 sec<br>0x1: 3 sec (default)<br>0x2: 4.5 sec<br>0x3: reserved | 2'b01   |
| 21  | 10[5]   |     | RESERVED                                                                                                                                                                                       |         |

### 6.21 Reserved Group MAC addresses

| PHY | MII    | R/W | Description                                                                                                                       | Default |
|-----|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 11[15] | R/W | PAUSE_FILTER<br><br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=1<br><br>1: forward<br>0: discard. (default),                | 1'b0    |
|     | 11[14] | R/W | RSVD_GMAC_FILTER_4<br><br>Reserved Group Address<br>01-80-c2-00-00-40 to FF<br><br>1: forward (default),<br>0: discard.           | 1'b1    |
|     | 11[13] | R/W | RSVD_GMAC_FILTER_3<br><br>Reserved Group Address<br>01-80-c2-00-00-30 to 3F<br><br>1: forward (default),<br>0: discard.           | 1'b1    |
|     | 11[12] | R/W | RSVD_GMAC_FILTER_2<br><br>Reserved Group Address<br>01-80-c2-00-00-22 to 2F<br><br>1: forward<br>0: discard (default)             | 1'b0    |
|     | 11[11] | R/W | RSVD_GMAC_FILTER_2<br><br>GVRP<br>GARP VLAN Registration Protocol<br>01-80-c2-00-00-21<br><br>1: forward<br>0: discard (default), | 1'b0    |

| PHY | MII    | R/W | Description                                                                                                                                          | Default |
|-----|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
|     | 11[10] | R/W | RSVD_GMAC_FILTER_2<br><br>GMRP<br>GARP Multicast Registration Protocol<br>01-80-c2-00-00-20<br><br>1: forward<br>0: discard (default)                | 1'b0    |
|     | 11[9]  | R/W | RSVD_GMAC_FILTER_1<br><br>Reserved Group Address<br>01-80-c2-00-00-10 to 1F<br><br>1: forward (default),<br>0: discard.                              | 1'b1    |
|     | 11[8]  | R/W | RSVD_GMAC_FILTER_1<br><br>ABM<br>All LANs Bridge Management Group address<br><br>1: forward<br>0: discard (default)                                  | 1'b0    |
|     | 11[7]  | R/W | RSVD_GMAC_FILTER_0<br><br>Reserved Group Address<br>01-80-c2-00-00-04 to 0F<br><br>1: forward<br>0: discard (default)                                | 1'b0    |
|     | 11[6]  | R/W | RSVD_GMAC_FILTER_0<br><br>LLDP<br>Std 802.1AB Link Layer Discovery Protocol address<br>01-80-C2-00-00-0E<br><br>1: forward (default),<br>0: discard. | 1'b1    |
|     | 11[5]  | R/W | RSVD_GMAC_FILTER_0<br><br>MVRP<br>Provider Bridge MVRP Address<br>01-80-C2-00-00-0D<br><br>1: forward<br>0: discard (default)                        | 1'b0    |

| PHY | MII       | R/W | Description                                                                                                                                                           | Default    |
|-----|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
|     | 11[4]     | R/W | RSVD_GMAC_FILTER_0<br><br>PBGA<br>Provider Bridge Group Address<br>01-80-C2-00-00-08<br><br>1: forward<br>0: discard (default)                                        | 1'b0       |
|     | 11[3]     | R/W | RSVD_GMAC_FILTER_0<br><br>802.1x<br>802.1x PAE Address<br>01-80-C2-00-00-03<br><br>1: forward (default),<br>0: discard.                                               | 1'b1       |
|     | 11[2]     | R/W | RSVD_GMAC_FILTER_0<br><br>SP<br>Slow Protocol (Link Aggregation and 802.3 OAM)<br>01-80-C2-00-00-02<br><br>1: forward (default),<br>0: discard.                       | 1'b1       |
|     | 11[1]     | R/W | RSVD_GMAC_FILTER_0<br><br>MAC_CTRL<br>MAC Control of Std IEEE 802.3<br>01-80-C2-00-00-01<br>(Not include PAUSE and 802.3ah)<br><br>1: forward<br>0: discard (default) | 1'b0       |
|     | 11[0]     | R/W | RSVD_GMAC_FILTER_0<br><br>BGA<br>Bridge Group Address<br>01-80-C2-00-00-00<br><br>1: forward (default),<br>0: discard.                                                | 1'b1       |
|     | 12[15:11] | R/W | RESERVED                                                                                                                                                              |            |
|     | 12[10:2]  |     | RSVD_FUTURE_0_FILTER<br>Reserved for Future Standardization 0<br><br>01-80-c2-00-00-04 to 0F<br><br>1: forward<br>0: discard (default)                                | 9'h<br>000 |

| PHY | MII      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Default      |
|-----|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
|     | 12[1]    | R/W | RSVD_MAC_CTRL_FILTER<br>Reserved MAC Control Opcode<br><br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=0x0007-0xffff<br><br>1: forward<br>0: discard (default)                                                                                                                                                                                                                                                                                                        | 1'b0         |
|     | 12[0]    | R/W | MPCP_FILTER<br>Multi-Poin Control Protocol<br><br>Five message as follows:<br>1. GATE<br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=2<br>2. REPORT<br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=3<br>3. REGISTER_REQ<br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=4<br>4. REGISTER<br>DA=individual MAC EtherType=0x8808 & Opcode=5<br>5. REGISTER_ACK<br>DA=01-80-c2-00-00-01 & EtherType=0x8808 & Opcode=6<br><br>1: forward<br>0: discard (default) | 1'b0         |
|     | 13[13:0] | R/W | RSVD_FUTURE_1_FILTER<br>Reserved for Future Standardization 1<br><br>01-80-c2-00-00-22 to 2F<br><br>1: forward<br>0: discard (default)                                                                                                                                                                                                                                                                                                                                     | 14'h<br>0000 |
|     | 14       | R/W | IEEE802.1ag_FILTER<br>IEEE 802.1ag Filter<br><br>01-80-c2-00-00-30 to 3F<br><br>1: forward (default),<br>0: discard.                                                                                                                                                                                                                                                                                                                                                       | 16'h<br>FFFF |

## 6.22 Switch control registers (II)

| PHY | MII      | R/W | Description                                                                                                                                                             | Default |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 21  | 30[15:8] | R/W | [15:14]: Reserved<br>[13]: DIFFSERV_EN<br>[12]: BF_FFFF_ONLY<br>1: broadcast DA=FFFFFFFF<br>0: broadcast DA=FFFFFFFF and multicast frame<br>[11:8]: special_add_forward | 8'h0d   |
|     | 30[7]    | R/W | FWD_MAC_CTL<br>Forward MAC control frame, the MAC control frame is identified by Ether/Type field (0x8808).<br>1: forward (default),<br>0: discard.                     | 1'b1    |
|     | 30[6:2]  |     | Reserved                                                                                                                                                                |         |
| 21  | 30[1:0]  | R/W | Drop extra long packet<br>Max forwarded packet length<br>2'b00: 1536 bytes (default)<br>2'b01: 1552 bytes<br>2'b10: 1518 bytes<br>2'b11: reserved                       | 2'b00   |

### 6.23 EEE Timing Parameter

| PHY | MII      | R/W | Description                                                                                                                                                                                                                                                             | Default |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 22  | 0[15:8]  |     | Reserved                                                                                                                                                                                                                                                                |         |
|     | 0[7:0]   | R/W | EEE_EN[7:0]<br>Energy Efficient Ethernet Enable for each port<br>bit[7]: Port 4 enable EEE function      Note 1<br>bit[6]: Port 3 enable EEE function<br>bit[4]: Port 2 enable EEE function<br>bit[3]: Port 1 enable EEE function<br>bit[2]: Port 0 enable EEE function | 8'hFF   |
|     | 1[15:14] | R/W | SLEEP_TIME_UNIT<br>Sleep Time Unit<br>0x0: 1s<br>0x1: 1ms<br>0x2: 1us                                                                                                                                                                                                   | 2'd2    |
|     | 1[11:0]  | R/W | SLEEP_TIME<br>The time to sleep = SLEEP_TIME_UNIT * SLEEP_TIME                                                                                                                                                                                                          | 12'd15  |
|     | 4[15:14] | R/W | WAKE_TIME_UNIT_P0<br>Wake Up Time Unit for Port 0<br>0x0: 1s<br>0x1: 1ms<br>0x2: 1us                                                                                                                                                                                    | 2'd2    |
|     | 4[11:0]  | R/W | WAKE_TIME_P0<br>Wake Up Time for Port 0<br>The time to wake = WAKE_TIME_UNIT_P0 * WAKE_TIME_P0<br>The time is between when switch de-assert LPI and when it can send data.                                                                                              | 12'd35  |
|     | 5[15:14] | R/W | WAKE_TIME_UNIT_P1<br>Wake Up Time Unit for Port 1                                                                                                                                                                                                                       | 2'd2    |
|     | 5[11:0]  | R/W | WAKE_TIME_P1<br>Wake Up Time for Port 1                                                                                                                                                                                                                                 | 12'd35  |
|     | 6[15:14] | R/W | WAKE_TIME_UNIT_P2<br>Wake Up Time Unit for Port 2                                                                                                                                                                                                                       | 2'd2    |
|     | 6[11:0]  | R/W | WAKE_TIME_P2<br>Wake Up Time for Port 2                                                                                                                                                                                                                                 | 12'd35  |
|     | 8[15:14] | R/W | WAKE_TIME_UNIT_P3<br>Wake Up Time Unit for Port 3                                                                                                                                                                                                                       | 2'd2    |
|     | 8[11:0]  | R/W | WAKE_TIME_P3<br>Wake Up Time for Port 3                                                                                                                                                                                                                                 | 12'd35  |
|     | 9[15:14] | R/W | WAKE_TIME_UNIT_P4<br>Wake Up Time Unit for Port 4                                                                                                                                                                                                                       | 2'd2    |
|     | 9[11:0]  | R/W | WAKE_TIME_P4<br>Wake Up Time for Port 4                                                                                                                                                                                                                                 | 12'd35  |

Note 1 : Port mapping refer Figure 2 Application Diagram

## 6.24 WOL (Wake on LAN)

| PHY | MII      | R/W | Description                                                       | Default  |
|-----|----------|-----|-------------------------------------------------------------------|----------|
| 22  | 10[15:8] | R/W | WOL_EN[7:0]<br>Wake on lan enable for each port                   | P(8'h00) |
|     | 10[7:2]  | R/W | RESERVED                                                          |          |
|     | 10[1:0]  | R/W | WOL_TIMER<br>0x0: disable<br>0x1: 3min<br>0x2: 5min<br>0x3: 10min | 2'b0     |

Note 1 : Port mapping refer Figure 2 Application Diagram

## 6.25 Link Aggregation

| PHY | MII      | R/W | Description                                                                                                                                                 | Default |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 22  | 11[15:5] |     | RESERVED                                                                                                                                                    |         |
|     | 11[4:3]  | R/W | AGGR_IDX_SEL<br>Aggregation Index Selection<br><br>2'b00: index[2:0]<br>2'b01: {index[3], index[1:0]}<br>2'b10: {index[3:2], index[0]}<br>2'b11: index[3:1] | 2'b00   |
|     | 11[2:0]  | R/W | AGGR_MODE<br>Aggregation Mode<br><br>3'b000: SMAC<br>3'b001: DMAC<br>3'b010: SMAC xor DMAC<br>3'b011: Source port                                           | 3'b000  |
|     | 12[7:0]  | R/W | AGGR_GROUP0<br>Aggregation Group 0                                                                                                                          | 8'h00   |
|     | 13[7:0]  | R/W | AGGR_GROUP1<br>Aggregation Group 1                                                                                                                          | 8'h00   |
|     | 16[7:0]  | R/W | AGGR_MASK0<br>Aggregation Port Mask 0<br>Only one port can be selected in each aggregation group                                                            | 8'hFF   |
|     | 17[7:0]  | R/W | AGGR_MASK1<br>Aggregation Port Mask 1                                                                                                                       | 8'hFF   |
|     | 18[7:0]  | R/W | AGGR_MASK2<br>Aggregation Port Mask 2                                                                                                                       | 8'hFF   |
|     | 20[7:0]  | R/W | AGGR_MASK3<br>Aggregation Port Mask 3                                                                                                                       | 8'hFF   |
|     | 21[7:0]  | R/W | AGGR_MASK4<br>Aggregation Port Mask 4                                                                                                                       | 8'hFF   |

## 6.26 VLAN Group Control Register

### 6.26.1 VLAN Classification

| PHY | MII     | R/W         | Description                                                                                                                                                                                                                                                                                                   | Default |
|-----|---------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 23  | 0[15]   | R/W<br>(SC) | VLAN_TABLE_CLR<br>Clear the contents of VLAN TABLE register<br>1: clear register<br>0: do nothing (default)<br>Self-clear after set and register cleared                                                                                                                                                      | 1'b0    |
|     | 0[14]   |             | RESERVED                                                                                                                                                                                                                                                                                                      |         |
|     | 0[13]   | R/W         | UNVID_MODE<br>Unknown-VID Mode<br>0: discard<br>1 : flood packet                                                                                                                                                                                                                                              | 1'b0    |
|     | 0[12:0] |             | RESERVED                                                                                                                                                                                                                                                                                                      |         |
|     | 1[15:8] | R/W         | VLAN_CLS[7:0]<br>VLAN Classification associated with each port<br>Only active at tagged-based VLAN<br>0 : use VID to classify VLAN<br>-use VID to search VLAN table if tag packet<br>-use PVID to search VLAN table if untag packet<br>1 : use PVID to classify VLAN<br>-always use PVID to search VLAN table | 8'h00   |
|     | 1[7:0]  |             | TAG_VLAN_EN<br>Tag-based VLAN enable                                                                                                                                                                                                                                                                          | 8'h00   |

### 6.26.2 VLAN Ingress Rule

| PHY | MII      | R/W | Description                                                                                                                                | Default |
|-----|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 23  | 2[15:14] |     | RESERVED                                                                                                                                   |         |
|     | 2[13]    | R/W | VLAN_DROP_CFI<br>Drop incoming frame, if the CFI field is not equal to zero.                                                               | 1'b0    |
|     | 2[12:10] | R/W | RSVD_VID[2:0]<br>Reserved VID                                                                                                              | 3'b001  |
|     |          |     | Bit 0<br>The null VID. If set, frames with null VID (priority-tagged frame) treat as untagged frames.<br>0: disable<br>1: enable (default) |         |
|     |          |     | Bit 1<br>VID=1 (default VID)<br>Replace default VID with PVID<br>0: disable (default)<br>1: enable                                         |         |
|     |          |     | Bit 2<br>VID=FFF<br>Discard frame if the VID is the value FFF<br>0: disable(default)<br>1: enable                                          |         |



| PHY | MII    | R/W | Description                                                                                                                                                                                                                     | Default |
|-----|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
|     | 2[9:8] | R/W | ACCEPTABLE_FRM_TYPE[1:0]<br>Acceptable Frame Type<br><br>2'b00 Admit all frames (default)<br>2'b01 Admit VLAN-tagged frames<br>2'b10 Admit Untagged frames<br>2'b11 Reserved                                                    | 2'b00   |
|     | 2[7:0] | R/W | VLAN_INGRESS_FILTER[7:0]<br>VLAN Ingress Filter associated with each port<br>If ingress filter for a given port is set, frame shall discard on that port whose VLAN classification does not include that port in it member set. | 8'hFF   |
| 23  | 3      |     | RESERVED                                                                                                                                                                                                                        |         |

### 6.26.3 Default VLAN Information

| PHY | MII      | R/W | Description                                                    | Default  |
|-----|----------|-----|----------------------------------------------------------------|----------|
| 23  | 7[15:0]  | R/W | VLAN_INFO_0.<br>Port 2 default VLAN information value (PVID_0) | 16'h0001 |
|     | 8[15:0]  | R/W | VLAN_INFO_1.<br>Port 3 default VLAN information value (PVID_1) | 16'h0001 |
|     | 9[15:0]  | R/W | VLAN_INFO_2.<br>Port 4 default VLAN information value (PVID_2) | 16'h0001 |
|     | 11[15:0] | R/W | VLAN_INFO_3.<br>Port 6 default VLAN information value (PVID_3) | 16'h0001 |
|     | 12[15:0] | R/W | VLAN_INFO_4.<br>Port 7 default VLAN information value (PVID_4) | 16'h0001 |

### 6.26.4 VLAN TAG Control Register

| PHY | MII     | R/W | Description                                                                                                                                 | Default |
|-----|---------|-----|---------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 23  | 13[7:0] | R/W | ADD_TAG[7:0] <i>Note 1</i><br>Port x adds a VLAN tag of each outgoing packet<br>Bit 0: Port0<br>Bit 1: Port1<br>...<br>Bit7: Port7          | 8'h00   |
|     | 14[7:0] | R/W | REMOVE_TAG[7:0] <i>Note 1</i><br>Port x removes the VLAN tag of each outgoing packet<br>Bit 0: Port0<br>Bit 1: Port1<br>...<br>Bit 7: Port7 | 8'h00   |

*Note 1* : Port mapping refer Figure 2 Application Diagram

### 6.26.5 Port Based VLAN Member Register

| PHY | MII      | R/W | Description                                                                                      | Default |
|-----|----------|-----|--------------------------------------------------------------------------------------------------|---------|
| 23  | 16[7:0]  | R/W | PBV_MEMBER_P0[7:0]<br>Port based VLAN member port<br>VLAN member port associated with the Port0. | 8'hFF   |
|     | 16[15:8] | R/W | PBV_MEMBER_P1[7:0]<br>Port based VLAN member port<br>VLAN member port associated with the Port1. | 8'hFF   |
|     | 17[7:0]  | R/W | PBV_MEMBER_P2[7:0]<br>Port based VLAN member port<br>VLAN member port associated with the Port2. | 8'hFF   |
|     | 18[7:0]  | R/W | PBV_MEMBER_P3[7:0]<br>Port based VLAN member port<br>VLAN member port associated with the Port3. | 8'hFF   |
|     | 18[15:8] | R/W | PBV_MEMBER_P4[7:0]<br>Port based VLAN member port<br>VLAN member port associated with the Port4. | 8'hFF   |

### 6.26.6 Leaky VLAN Control Register

| PHY | MII      | R/W | Description                                                                                                                                             | Default |
|-----|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 23  | 19[15:3] |     | RESERVED                                                                                                                                                |         |
|     | 19[2:0]  | R/W | LEAKY_VLAN[2:0]<br>Bit0: ARP leaky VLAN<br>Bit1: Unicast forwarding leaky VLAN, DA=individual MAC & DA match<br>was found<br>Bit2: Multicast leaky VLAN | 2'b00   |

## 6.27 VLAN Table

### 6.27.1 VLAN Control Register

| PHY | MII     | R/W | Description                                                                                              | Default      |
|-----|---------|-----|----------------------------------------------------------------------------------------------------------|--------------|
| 24  | 0[15:0] | R/W | VLAN_VALID[15:0]<br>VALN filter is valid.<br>The VALN filter entry X is valid associated with the VID_X. | 16'h<br>0000 |

### 6.27.2 VLAN Identifier Register

| PHY | MII     | R/W | Description                                            | Default |
|-----|---------|-----|--------------------------------------------------------|---------|
| 24  | 1[11:0] | R/W | VID_0[11:0]<br>VLAN identifier associated with VALN 0. | 12'h001 |
|     | 2[11:0] | R/W | VID_1[11:0]<br>VLAN identifier associated with VALN 1. | 12'h002 |
|     | 3[11:0] | R/W | VID_2[11:0]<br>VLAN identifier associated with VALN 2. | 12'h003 |
|     | 4[11:0] | R/W | VID_3[11:0]<br>VLAN identifier associated with VALN 3. | 12'h004 |
|     | 5[11:0] | R/W | VID_4[11:0]<br>VLAN identifier associated with VALN 4. | 12'h005 |

| PHY | MII      | R/W | Description                                            | Default |
|-----|----------|-----|--------------------------------------------------------|---------|
|     | 6[11:0]  | R/W | VID_5[11:0]<br>VLAN identifier associated with VALN 5. | 12'h006 |
|     | 7[11:0]  | R/W | VID_6[11:0]<br>VLAN identifier associated with VALN 6. | 12'h007 |
|     | 8[11:0]  | R/W | VID_7[11:0]<br>VLAN identifier associated with VALN 7. | 12'h008 |
|     | 9[11:0]  | R/W | VID_8[11:0]<br>VLAN identifier associated with VALN 8. | 12'h009 |
|     | 10[11:0] | R/W | VID_9[11:0]<br>VLAN identifier associated with VALN 9. | 12'h00A |
|     | 11[11:0] | R/W | VID_A[11:0]<br>VLAN identifier associated with VALN A. | 12'h00B |
|     | 12[11:0] | R/W | VID_B[11:0]<br>VLAN identifier associated with VALN B. | 12'h00C |
|     | 13[11:0] | R/W | VID_C[11:0]<br>VLAN identifier associated with VALN C. | 12'h00D |
|     | 14[11:0] | R/W | VID_D[11:0]<br>VLAN identifier associated with VALN D. | 12'h00E |
|     | 15[11:0] | R/W | VID_E[11:0]<br>VLAN identifier associated with VALN E. | 12'h00F |
|     | 16[11:0] | R/W | VID_F[11:0]<br>VLAN identifier associated with VALN F. | 12'h010 |

### 6.27.3 VLAN Member Register

| PHY | MII      | R/W | Description                                                                           | Default |
|-----|----------|-----|---------------------------------------------------------------------------------------|---------|
| 24  | 17[7:0]  | R/W | VLAN_MEMBER_0[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_0. | 8'hFF   |
|     | 17[15:8] | R/W | VLAN_MEMBER_1[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_1. | 8'hFF   |
|     | 18[7:0]  | R/W | VLAN_MEMBER_2[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_2. | 8'hFF   |
|     | 18[15:8] | R/W | VLAN_MEMBER_3[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_3. | 8'hFF   |
|     | 19[7:0]  | R/W | VLAN_MEMBER_4[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_4. | 8'hFF   |
|     | 19[15:8] | R/W | VLAN_MEMBER_5[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_5. | 8'hFF   |
|     | 20[7:0]  | R/W | VLAN_MEMBER_6[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_6. | 8'hFF   |



| PHY | MII      | R/W | Description                                                                           | Default |
|-----|----------|-----|---------------------------------------------------------------------------------------|---------|
|     | 20[15:8] | R/W | VLAN_MEMBER_7[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_7. | 8'hFF   |
|     | 21[7:0]  | R/W | VLAN_MEMBER_8[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_8. | 8'hFF   |
|     | 21[15:8] | R/W | VLAN_MEMBER_9[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_9. | 8'hFF   |
|     | 22[7:0]  | R/W | VLAN_MEMBER_A[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_A. | 8'hFF   |
|     | 22[15:8] | R/W | VLAN_MEMBER_B[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_B. | 8'hFF   |
|     | 23[7:0]  | R/W | VLAN_MEMBER_C[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_C. | 8'hFF   |
|     | 23[15:8] | R/W | VLAN_MEMBER_D[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_D. | 8'hFF   |
|     | 24[7:0]  | R/W | VLAN_MEMBER_E[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_E. | 8'hFF   |
|     | 24[15:8] | R/W | VLAN_MEMBER_F[7:0]<br>VLAN member port<br>VLAN member port associated with the VID_F. | 8'hFF   |

## 7 Electrical Characteristics

### 7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

|                                                |                 |
|------------------------------------------------|-----------------|
| Supply Voltage                                 | – 0.3V to 3.63V |
| Input Voltage                                  | – 0.3V to 3.63V |
| Output Voltage                                 | – 0.3V to 3.63V |
| Storage Temperature                            | – 65°C to 150°C |
| Ambient Operating Temperature (Ta) (IP175G/GH) | 0°C to 70°C     |
| IC Junction Temperature (Tj) (IP175G/GH)       | 0°C to 125°C    |
| Ambient Operating Temperature (Ta) (IP175GHI)  | –40°C to 85°C   |
| IC Junction Temperature (Tj) (IP175GHI)        | –40°C to 125°C  |

### 7.2 Crystal Specifications

| Item | Parameter                    | Range                 |
|------|------------------------------|-----------------------|
| 1    | Nominal Frequency            | 25.000 MHz            |
| 2    | Oscillation Mode             | Fundamental Mode      |
| 3    | Frequency Tolerance at 25°C  | +/- 50 ppm            |
| 4    | Temperature Characteristics  | +/- 50 ppm            |
| 5    | Operating Temperature Range  | –10°C ~ +70°C         |
| 6    | Equivalent Series Resistance | 40 ohm Max.           |
| 7    | Drive Level                  | 100 $\mu$ W           |
| 8    | Load Capacitance             | 20 pF                 |
| 9    | Shunt Capacitance            | 7 pF Max              |
| 10   | Insulation Resistance        | Mega ohm Min./DC 100V |
| 11   | Aging Rate A Year            | +/- 5 ppm/year        |

### 7.3 DC Characteristic

#### Operating Conditions

| Parameter                  | Sym.                | Min. | Typ. | Max. | Unit | Conditions                    |
|----------------------------|---------------------|------|------|------|------|-------------------------------|
| Core Supply Voltage        | DVDD                | 1.05 | 1.1  | 1.23 | V    |                               |
| Analog Low Supply Voltage  | AV10                |      |      |      |      |                               |
| LDO drop voltage           | V <sub>LDODRP</sub> |      | 1.0  | 1.3  |      |                               |
| Analog High Supply Voltage | AV33                | 3    | 3.3  | 3.6  |      |                               |
| I/O Pad Supply Voltage     | PVDD                |      |      |      |      |                               |
| LDO output current         | I <sub>LDO</sub>    |      |      | 130  | mA   |                               |
| Power Consumption          | P <sub>100MF</sub>  |      | 520  |      | mW   | All port link 100M Full activ |
|                            | P <sub>10MF</sub>   |      | 488  |      |      | All port link 10M Full activ  |
|                            | P <sub>IDLE</sub>   |      | 125  |      |      | All port unlink               |

#### Input Clock

| Parameter           | Sym.           | Min. | Typ. | Max. | Unit | Conditions |
|---------------------|----------------|------|------|------|------|------------|
| Frequency           | F              |      | 25   |      | MHz  |            |
| Frequency Tolerance | F <sub>T</sub> | –50  |      | +50  | PPM  |            |

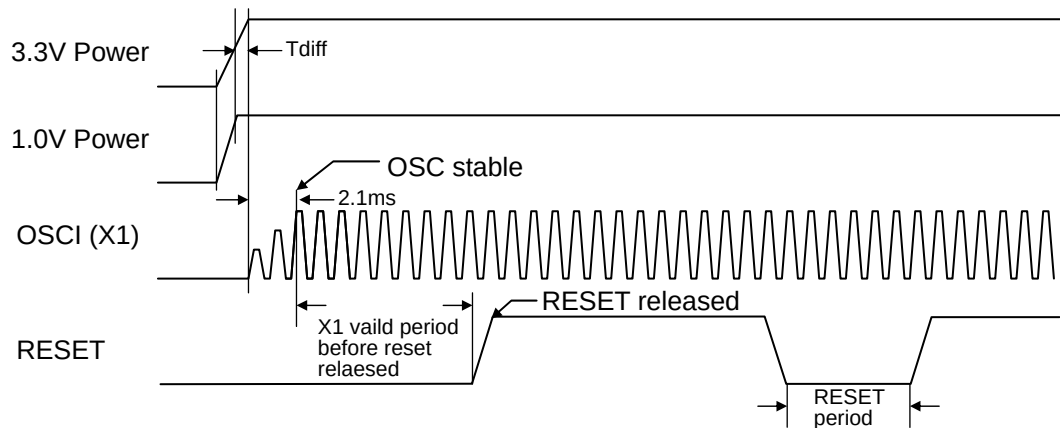
## I/O Electrical Characteristics

| Parameter                                                                           | Sym        | Min.                               | Max.                               | Unit | Conditions |
|-------------------------------------------------------------------------------------|------------|------------------------------------|------------------------------------|------|------------|
| Input Low Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD  | $V_{IL}$   |                                    | 0.39*PVDD<br>0.36*PVDD<br>0.4*PVDD | V    |            |
| Input High Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD | $V_{IH}$   | 0.58*PVDD<br>0.58*PVDD<br>0.6*PVDD |                                    |      |            |
| X1 Input Low Voltage                                                                | $V_{ILX1}$ |                                    | 0.6                                |      |            |
| X1 Input High Voltage                                                               | $V_{IHX1}$ | 1.5                                |                                    |      |            |
| Output Low Voltage                                                                  | $V_{OL}$   |                                    | 0.4                                |      |            |
| Output High Voltage                                                                 | $V_{OH}$   | 2.4                                |                                    |      |            |
| RESETB Threshold Voltage                                                            | $V_{RST}$  | 0.4*PVDD                           | 0.6*PVDD                           |      |            |

## 7.4 AC Timing

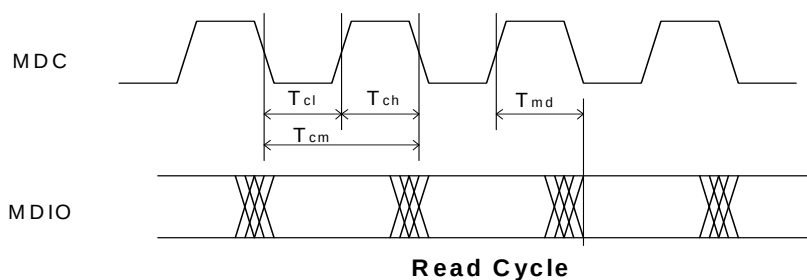
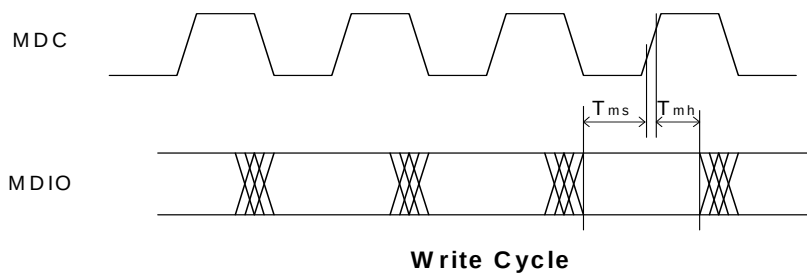
### 7.4.1 Power On Sequence and Reset Timing

| Description                                              | Min. | Typ. | Max. | Unit |
|----------------------------------------------------------|------|------|------|------|
| X1 valid period before reset released                    | 10   | -    | -    | ms   |
| Reset period                                             | 10   | -    | -    | ms   |
| All power source ready before reset released             | 10   |      |      | ms   |
| Time difference between VCC3.3 and VCC1.0 ( $T_{diff}$ ) | -2   |      |      | ms   |



# Serial Management Interface Timing

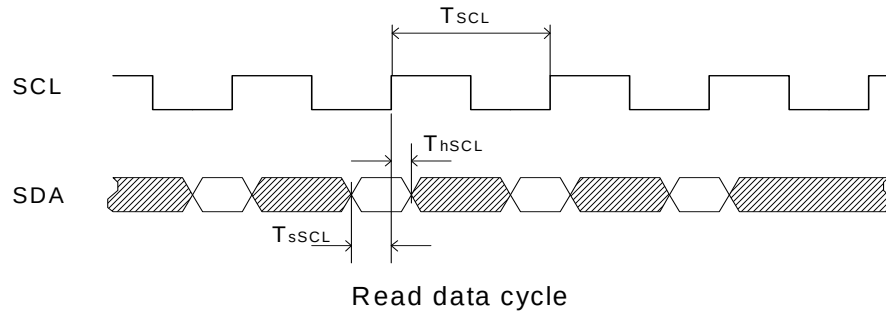
| Symbol   | Description       | Min. | Typ. | Max. | Unit |
|----------|-------------------|------|------|------|------|
| $T_{ch}$ | MDC High Time     | 200  | -    | -    | ns   |
| $T_{cl}$ | MDC Low Time      | 200  | -    | -    | ns   |
| $T_{cm}$ | MDC period        | 400  | -    | -    | ns   |
| $T_{md}$ | MDIO output delay | 5    | -    | 20   | ns   |
| $T_{mh}$ | MDIO setup time   | 10   | -    | -    | ns   |
| $T_{ms}$ | MDIO hold time    | 10   | -    | -    | ns   |



## 7.4.2 EEPROM Timing

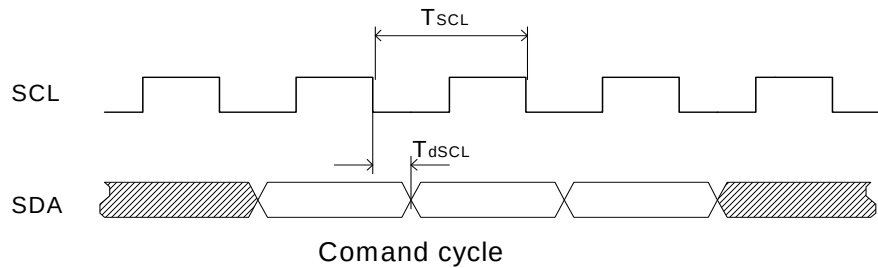
### 7.4.2.1 Data read cycle

| Symbol     | Description           | Min. | Typ.  | Max. | Unit |
|------------|-----------------------|------|-------|------|------|
| $T_{SCL}$  | Receive clock period  | -    | 20480 | -    | ns   |
| $T_{sSCL}$ | SDA to SCL setup time | 2    | -     | -    | ns   |
| $T_{hSCL}$ | SDA to SCL hold time  | 0.5  | -     | -    | ns   |



### 7.4.2.2 Command cycle

| Symbol     | Description             | Min. | Typ.  | Max. | Unit |
|------------|-------------------------|------|-------|------|------|
| $T_{SCL}$  | Transmit clock period   | -    | 20480 | -    | ns   |
| $T_{dSCL}$ | SCL falling edge to SDA | -    | -     | 5200 | ns   |



## 7.5 Thermal Data

| Theta Ja  | Theta Jc  | Conditions  | Units |
|-----------|-----------|-------------|-------|
| 30.7~32.5 | 11.6~12.4 | 2 Layer PCB | °C/W  |
| 25.0~26.6 | 11.1~11.7 | 4 Layer PCB | °C/W  |



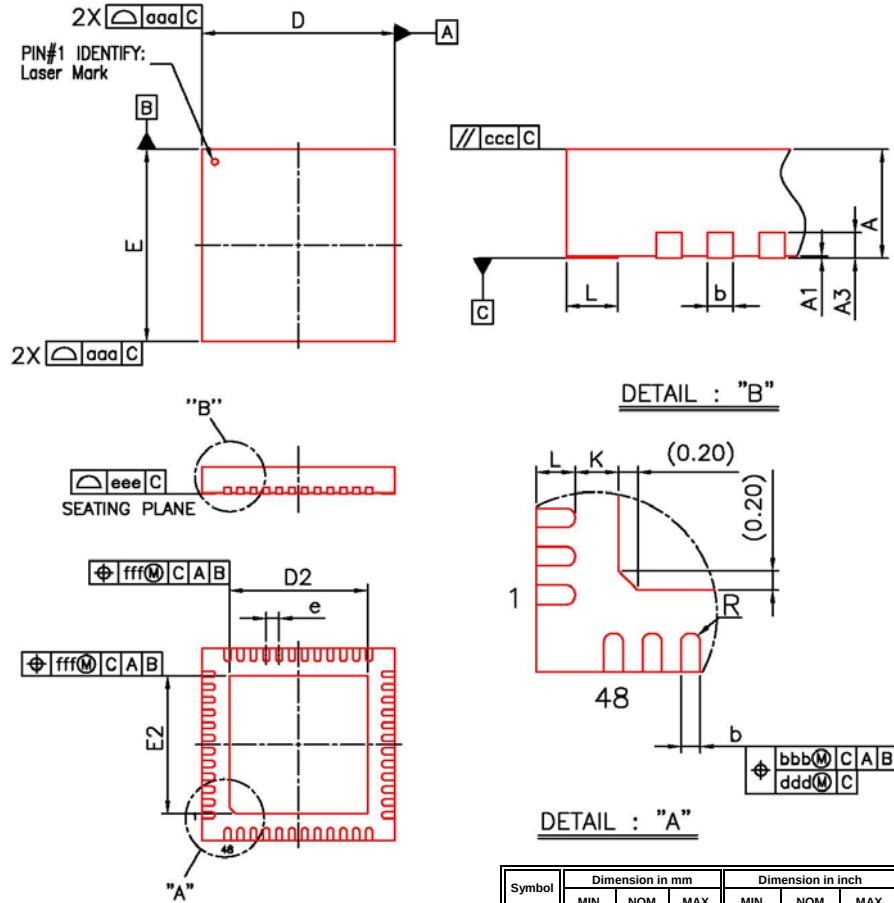
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**8 Order Information**

| Part No.  | Package     | Operating Temperature | Notice |
|-----------|-------------|-----------------------|--------|
| IP175G/GH | 48-Lead QFN | 0°C to 70°C           |        |
| IP175GHI  | 48-Lead QFN | -40°C to 85°C         |        |

## 9 Package Detail

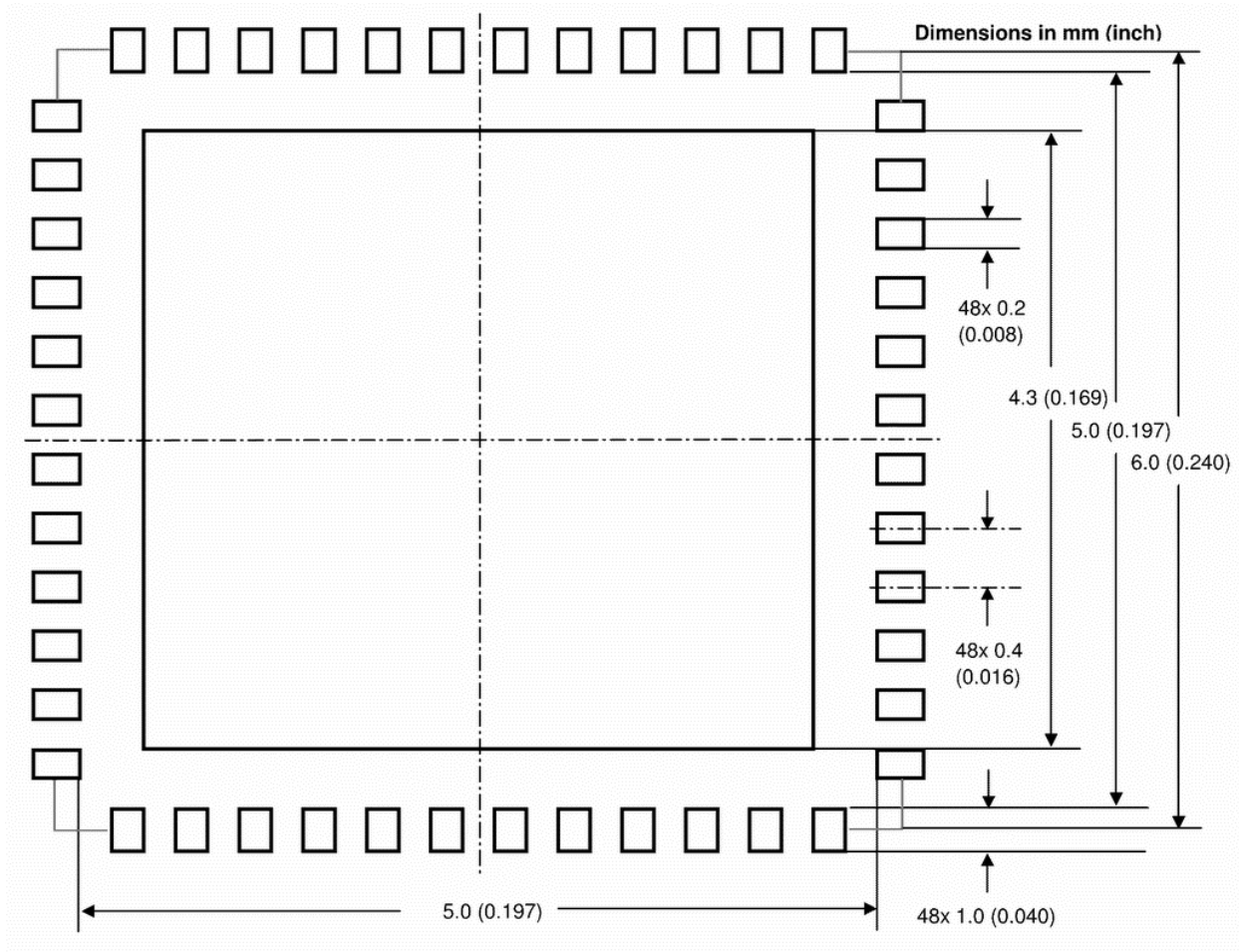
### 9.1 48 QFN Outline Dimensions



| Symbol | Dimension in mm |      |      | Dimension in inch |       |       |
|--------|-----------------|------|------|-------------------|-------|-------|
|        | MIN             | NOM  | MAX  | MIN               | NOM   | MAX   |
| A      | 0.80            | 0.85 | 0.90 | 0.031             | 0.033 | 0.035 |
| A1     | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A3     | 0.20 REF        |      |      | 0.008 REF         |       |       |
| b      | 0.15            | 0.20 | 0.25 | 0.006             | 0.008 | 0.010 |
| D/E    | 5.90            | 6.00 | 6.10 | 0.232             | 0.236 | 0.240 |
| D2/E2  | 4.15            | 4.30 | 4.45 | 0.163             | 0.169 | 0.175 |
| e      | 0.40 BSC        |      |      | 0.016 BSC         |       |       |
| L      | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |
| K      | 0.20            | ---  | ---  | 0.008             | ---   | ---   |
| R      | 0.075           | ---  | ---  | 0.003             | ---   | ---   |
| aaa    | 0.10            |      |      | 0.004             |       |       |
| bbb    | 0.07            |      |      | 0.003             |       |       |
| ccc    | 0.10            |      |      | 0.004             |       |       |
| ddd    | 0.05            |      |      | 0.002             |       |       |
| eee    | 0.08            |      |      | 0.003             |       |       |
| fff    | 0.10            |      |      | 0.004             |       |       |

Note:

1. CONTROLLING DIMENSION: MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO - 220.

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