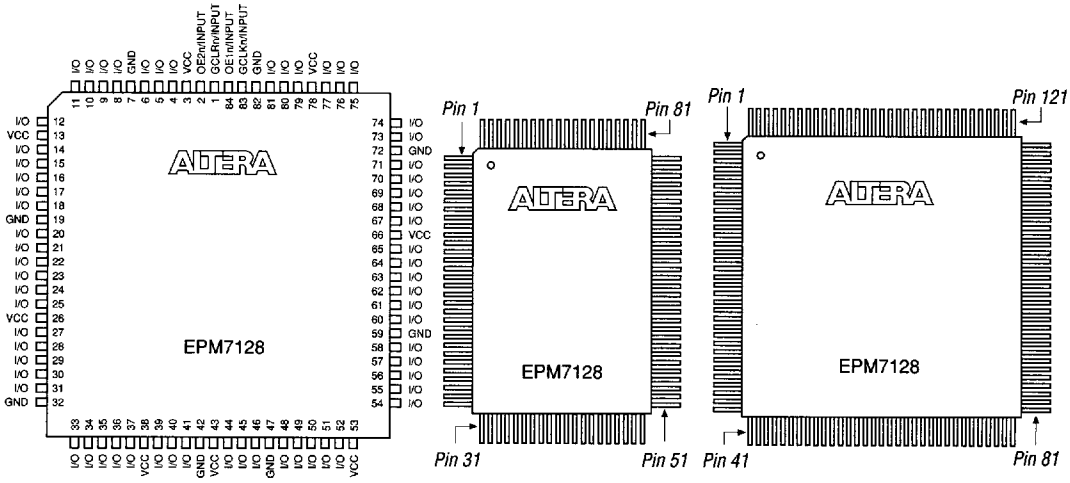
EPM7128 EPLD

Features

- High-density CMOS EPLD based on second-generation MAX architecture
  - 2,500 usable gates
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 100 inputs or 96 outputs
- 128 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in the following packages (see Figure 22):
  - 84-pin plastic J-lead chip carrier (PLCC)
  - 100- and 160-pin plastic quad flat pack (PQFP)

Figure 22. EPM7128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 7 and 8 in this data sheet for pin-out information.



84-Pin J-Lead 100-Pin QFP 160-Pin QFP

General Description

The Altera EPM7128 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 23. Fabricated on a 0.8-micron EEPROM technology, the EPM7128 provides 2,500 usable gates, counter speeds of 100 MHz, and propagation delays of 10 ns. The EPM7128 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 128 macrocells,

the EPM7128 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7128 provides FPGA density with PAL performance. The high density and high I/O pin count make the EPM7128 appropriate for prototyping gate arrays. The EPM7128 can also accommodate both logic- and I/O-intensive designs.

Figure 23. EPM7128 Block Diagram

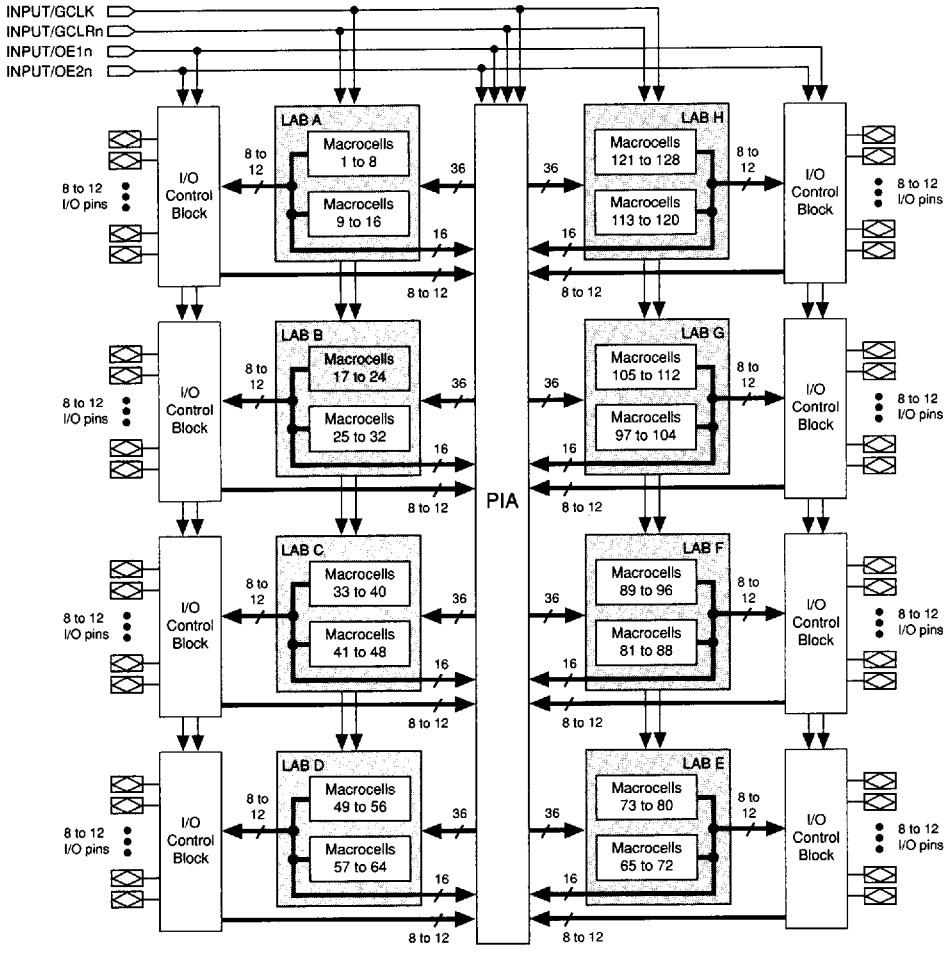


Figure 24 shows the output drive characteristics of EPM7128 I/O pins.

Figure 24. EPM7128 Output Drive Characteristics

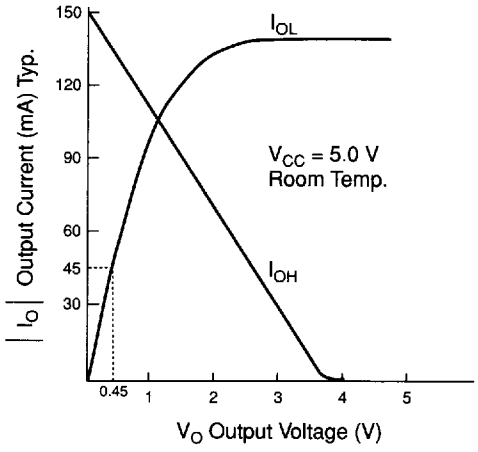


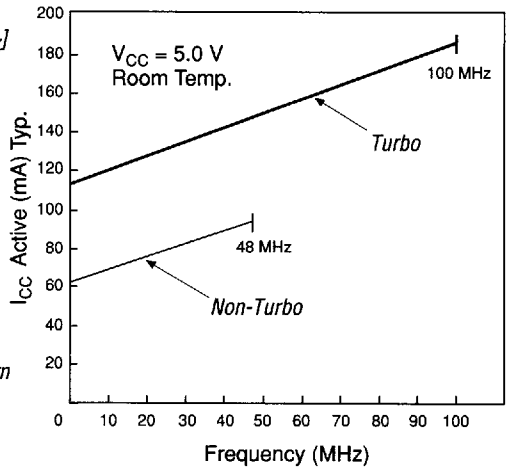
Figure 25 shows typical supply current versus frequency for the EPM7128.

Figure 25. EPM7128 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.91 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0053 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Rating

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	-40	85	° C
T_C	Case temperature	For military use	-55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions

Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		90		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		100		mA

Capacitance

Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7128-10		EPM7128-12		EPM7128-15		EPM7128-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-reg. output	C1 = 35 pF		10		12		15		20	ns
t_{PD2}	I/O input to non-reg. output			10		12		15		20	ns
t_{SU}	Global clock setup time		8		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		6		8		12	ns
t_{CH}	Global clock high time		4		4		5		6		ns
t_{CL}	Global clock low time		4		4		5		6		ns
t_{ASU}	Array clock setup time		3		4		4		5		ns
t_{AH}	Array clock hold time		3		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12		15		20	ns
t_{ACH}	Array clock high time		4		5		6		8		ns
t_{ACL}	Array clock low time		4		5		6		8		ns
t_{CNT}	Minimum global clock period			10		11		13		16	ns
f_{CNT}	Max. int. global clock freq.	*Note (4)*	100		90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			10		11		13		16	ns
f_{ACNT}	Max. int. array clock freq.	*Note (4)*	100		90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		125		100		83.3		MHz

Internal Timing Parameters			EPM7128-10		EPM7128-12		EPM7128-15		EPM7128-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad & buffer delay			1		2		2		3	ns
t_{IO}	I/O input pad & buffer delay			1		2		2		3	ns
t_{SEXP}	Shared expander delay			5		7		8		9	ns
t_{PEXP}	Parallel expander delay			0.8		1		1		2	ns
t_{LAD}	Logic array delay			5		5		6		8	ns
t_{LAC}	Logic control array delay			5		5		6		8	ns
t_{OD}	Output buffer & pad delay	C1 = 35 pF		2		3		4		5	ns
t_{ZX}	Output buffer enable delay			5		6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		6		9	ns
t_{SU}	Register setup time		3		4		4		4		ns
t_{H}	Register hold time		3		4		4		5		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			5		5		6		8	ns
t_{EN}	Register enable time			5		5		6		8	ns
t_{GLOB}	Global control delay			1		0		1		3	ns
t_{PRE}	Register preset time			3		3		4		4	ns
t_{CLR}	Register clear time			3		3		4		4	ns
t_{PIA}	Prog. Interconn. Array delay			1		1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		11		12		13		15	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7128-10, EPM7128-12, EPM7128-15, EPM7128-20
Industrial Temp.	(–40° C to 85° C)	EPM7128-20
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7128 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7128-1	EPM7128-10
EPM7128-2	EPM7128-12
EPM7128-3	EPM7128-15
EPM7128-4	EPM7128-20

Pin-Out Information

Tables 7 and 8 provide pin-out information for the EPM7128 packages.

Table 7. EPM7128 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	91	141
OE1n	84	90	140
OE2n	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)	–	–	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 8. EPM7128 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	–	4	160	17	B	22	16	21
2	A	–	–	–	18	B	–	–	–
3	A	12	3	159	19	B	21	15	20
4	A	–	–	158	20	B	–	–	19
5	A	11	2	153	21	B	20	14	18
6	A	10	1	152	22	B	–	12	16
7	A	–	–	–	23	B	–	–	–
8	A	9	100	151	24	B	18	11	15
9	A	–	99	150	25	B	17	10	14
10	A	–	–	–	26	B	–	–	–
11	A	8	98	149	27	B	16	9	13
12	A	–	–	147	28	B	–	–	12
13	A	6	96	146	29	B	15	8	11
14	A	5	95	145	30	B	–	7	10
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	14	6	9
33	C	–	27	41	49	D	41	39	59
34	C	–	–	–	50	D	–	–	–
35	C	31	26	33	51	D	40	38	58
36	C	–	–	32	52	D	–	–	57
37	C	30	25	31	53	D	39	37	56
38	C	29	24	30	54	D	–	35	54
39	C	–	–	–	55	D	–	–	–
40	C	28	23	29	56	D	37	34	53
41	C	–	22	28	57	D	36	33	52
42	C	–	–	–	58	D	–	–	–
43	C	27	21	27	59	D	35	32	51
44	C	–	–	25	60	D	–	–	50
45	C	25	19	24	61	D	34	31	49
46	C	24	18	23	62	D	–	30	48
47	C	–	–	–	63	D	–	–	–
48	C	23	17	22	64	D	33	29	43

Table 8. EPM7128 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	44	42	62	81	F	–	54	80
66	E	–	–	–	82	F	–	–	–
67	E	45	43	63	83	F	54	55	88
68	E	–	–	64	84	F	–	–	89
69	E	46	44	65	85	F	55	56	90
70	E	–	46	67	86	F	56	57	91
71	E	–	–	–	87	F	–	–	–
72	E	48	47	68	88	F	57	58	92
73	E	49	48	69	89	F	–	59	93
74	E	–	–	–	90	F	–	–	–
75	E	50	49	70	91	F	58	60	94
76	E	–	–	71	92	F	–	–	96
77	E	51	50	72	93	F	60	62	97
78	E	–	51	73	94	F	61	63	98
79	E	–	–	–	95	F	–	–	–
80	E	52	52	78	96	F	62	64	99
97	G	63	65	100	113	H	–	77	121
98	G	–	–	–	114	H	–	–	–
99	G	64	66	101	115	H	73	78	122
100	G	–	–	102	116	H	–	–	123
101	G	65	67	103	117	H	74	79	128
102	G	–	69	105	118	H	75	80	129
103	G	–	–	–	119	H	–	–	–
104	G	67	70	106	120	H	76	81	130
105	G	68	71	107	121	H	–	82	131
106	G	–	–	–	122	H	–	–	–
107	G	69	72	108	123	H	77	83	132
108	G	–	–	109	124	H	–	–	134
109	G	70	73	110	125	H	79	85	135
110	G	–	74	111	126	H	80	86	136
111	G	–	–	–	127	H	–	–	–
112	G	71	75	112	128	H	81	87	137