TEXAS INSTRUMENTS

DAC8551

SLAS429C – APRIL 2005 – REVISED MARCH 2016

DAC8551 16-Bit, Ultralow-Glitch, Voltage-Output Digital-to-Analog Converter

1 Features

- Relative Accuracy: 3LSB
- Glitch Energy: 0.1 nV-s
- *Micro*Power Operation: 140 µA at 2.7 V
- Power-On Reset to Zero
- Power Supply: 2.7 V to 5.5 V
- 16-Bit Monotonic Over Temperature
- Settling Time: 10 µs to ±0.003% FSR
- Low-Power Serial Interface with Schmitt-Triggered Inputs
- On-Chip Output Buffer Amplifier with Rail-to-Rail Operation
- Power-Down Capability
- Binary Input
- $\overline{\text{SYNC}}$ Interrupt Facility
- Drop-In Compatible With DAC85x1 and DAC8550 (2's Complement Input)

2 Applications

- Process Control
- Data Acquisition Systems
- Closed-Loop Servo-Control
- PC Peripherals
- Portable Instrumentation
- Programmable Attenuation

3 Description

The DAC8551 is a small, low-power, voltage output, 16-bit digital-to-analog converter (DAC). It is monotonic, provides good linearity, and minimizes undesired code-to-code transient voltages. The DAC8551 uses a versatile 3-wire serial interface that operates at clock rates to 30 MHz and is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC8551 requires an external reference voltage to set its output range. The DAC8551 incorporates a power-on-reset circuit that ensures the DAC output powers up at 0 V and remains there until a valid write takes place to the device. The DAC8551 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200 nA at 5 V.

The low-power consumption of this device in normal operation makes it ideally suited for portable, battery-operated equipment. The power consumption is 0.38 mW at 2.7 V, reducing to less than 1 µW in power-down mode.

For additional flexibilty, see the DAC8550 (SLAS476), a 2's complement-input counterpart to the DAC8551.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8551	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram

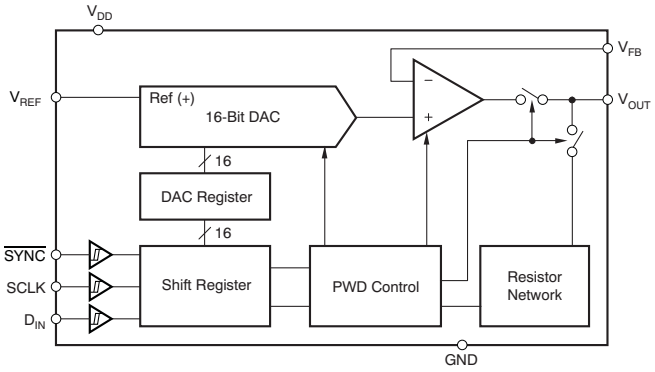


Table of Contents

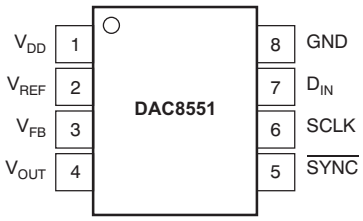
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2006) to Revision C	Page
• Removed *Packaging/Ordering Information* table	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D_{IN}	7	I	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
GND	8	GND	Ground reference point for all circuitry on the part
SCLK	6	I	Serial clock input. Data can be transferred at rates up to 30-MHz Schmitt-Trigger logic input.
$\overline{SYNC}$	5	I	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8551). Schmitt-Trigger logic input.
V_{DD}	1	PWR	Power supply input, 2.7 V to 5.5 V
V_{FB}	3	I	Feedback connection for the output amplifier. For voltage output operation, tie to V_{OUT} externally.
V_{OUT}	4	O	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
V_{REF}	2	I	Reference voltage input

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Input voltage	GND	–0.3	6	V
Digital input voltage	GND	–0.3	V_{DD} + 0.3	V
Output voltage	GND	–0.3	V_{DD} + 0.3	V
Operating temperature		–40	105°C	°C
Junction temperature, T_J			150°C	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage (V_{DD} to GND)	2.7		5.5	V
	Digital input voltage (D_{IN}, SCLK, and $\overline{SYNC}$)	0		V_{DD}	V
V_{REF}	Reference input voltage	0		V_{DD}	V
V_{FB}	Output amplifier feedback input		V_{OUT}		V
T_A	Operating ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC (1)		DAC8551 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V and –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE (1)							
	Resolution			16			Bits
	Relative accuracy	Measured by line passing through codes 485 and 64741	DAC8551		±3	±8	LSB
			DAC8551A		±3	±12	LSB
	Differential nonlinearity	16-bit monotonic			±0.25	±1	LSB
	Zero-code error	Measured by line passing through codes 485 and 64741			±2	±12	mV
	Full-scale error				±0.05%	±0.5%	FSR
	Gain error	Measured by line passing through codes 485 and 64741	DAC8551		±0.02%	±0.15%	FSR
			DAC8551A		±0.02%	±0.2%	FSR
	Zero-code error drift				±5		µV/°C
	Gain temperature coefficient				±1		ppm of FSR/°C
PSRR	Power-supply rejection ratio	R_L = 2 kΩ, C_L = 200 pF			0.75		mV/V
OUTPUT CHARACTERISTICS (2)							
	Output voltage range			0		V_{REF}	V
	Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2 kΩ, 0 pF < C_L < 200 pF			8	10	µs
		R_L = 2 kΩ, C_L = 50 pF			12		µs
	Slew rate				1.8		V/µs
	Capacitive load stability	R_L = ∞			470		pF
		R_L = 2 kΩ			1000		pF
	Code change glitch impulse	1 LSB change around major carry			0.1		nV-s
	Digital feedthrough	50 kΩ series resistance on digital lines			0.1		
	DC output impedance	At mid-code input			1		Ω
	Short-circuit current	V_{DD} = 5 V			50		mA
		V_{DD} = 3 V			20		
	Power-up time	Coming out of power-down mode, V_{DD} = 5 V			2.5		µs
		Coming out of power-down mode, V_{DD} = 3 V			5		
AC PERFORMANCE							
SNR	Signal-to-noise ratio	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			95		dB
THD	Total harmonic distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			–85		dB
SFDR	Spurious-free dynamic range	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			87		dB
SINAD	Signal to noise and distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			84		dB
REFERENCE INPUT							
	Reference current	V_{REF} = V_{DD} = 5 V			40	75	µA
		V_{REF} = V_{DD} = 3.6 V			30	45	µA
	Reference input range			0		V_{DD}	V
	Reference input impedance				125		kΩ
LOGIC INPUTS (2)							
	Input current				±1		µA
$V_{IN}L$	Input LOW voltage	V_{DD} = 5 V				0.8	V
		V_{DD} = 3 V				0.6	
$V_{IN}H$	Input HIGH voltage	V_{DD} = 5 V		2.4			V
		V_{DD} = 3 V		2.1			
	Pin capacitance					3	pF

(1) Linearity calculated using a reduced code range of 485 to 64741; output unloaded.
(2) Specified by design and characterization; not production tested.

Electrical Characteristics (continued)

V_{DD} = 2.7 V to 5.5 V and –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER REQUIREMENTS							
V_{DD}	Supply voltage			2.7		5.5	V
I_{DD}	Supply current	Normal mode, input code = 32768, no load, does not include reference current	V_{DD} = 3.6 V to 5.5 V, V_{IH} = V_{DD} and V_{IL} = GND		160	250	µA
			V_{DD} = 2.7 V to 3.6 V, V_{IH} = V_{DD} and V_{IL} = GND		140	240	
		All power-down modes, V_{IH} = V_{DD} and V_{IL} = GND	V_{DD} = 3.6 V to 5.5 V		0.2	2	µA
			V_{DD} = 2.7 V to 3.6 V		0.05	2	
I_{OUT}/I_{DD}	Power efficiency	I_{LOAD} = 2 mA, V_{DD} = 5 V			89%		
	Specified performance temperature			–40		105	°C

6.6 Timing Characteristics

V_{DD} = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1(3)	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	33			
t_2	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	13			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_3	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	22.5			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_5	Data setup time	V_{DD} = 2.7 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	V_{DD} = 2.7 V to 3.6 V	4.5			ns
		V_{DD} = 3.6 V to 5.5 V	4.5			
t_7	24th SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	33			
t_9	24th SCLK falling edge to $\overline{SYNC}$ falling edge	V_{DD} = 2.7 V to 5.5 V	100			ns

(1) All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) See Figure 1.
(3) Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

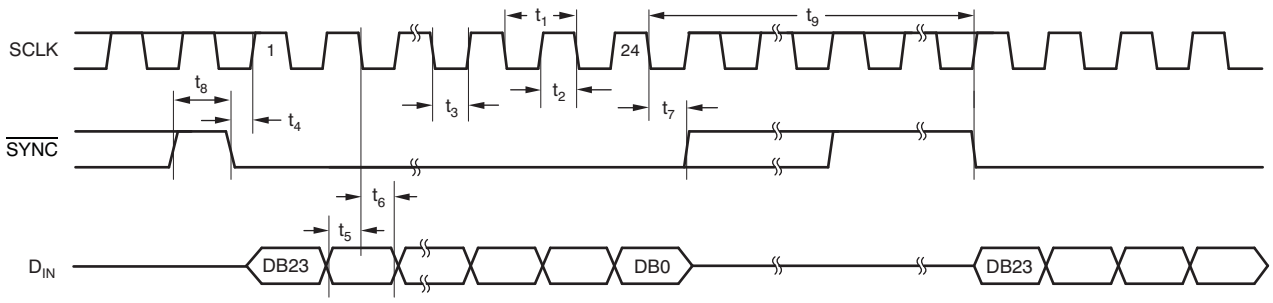


Figure 1. Serial Write Operation

6.7 Typical Characteristics

6.7.1 V_{DD} = 5 V

At T_A = 25°C (unless otherwise noted)

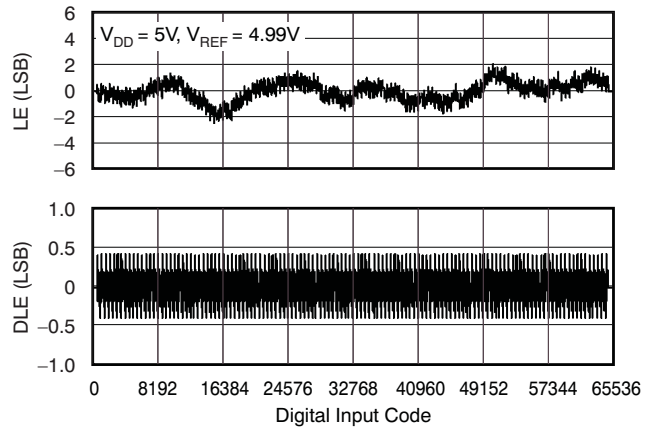


Figure 2. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

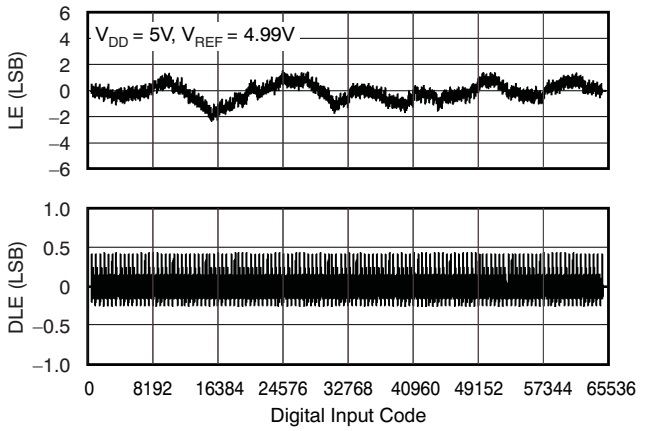


Figure 3. Linearity Error and Differential Linearity Error vs Digital Input Code

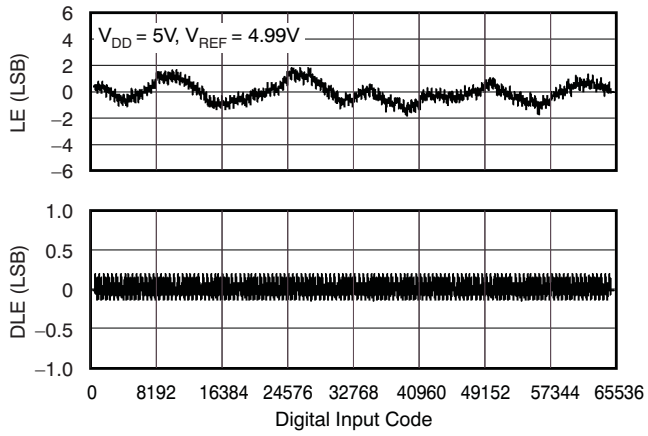


Figure 4. Linearity Error and Differential Linearity Error vs Digital Input Code (105°C)

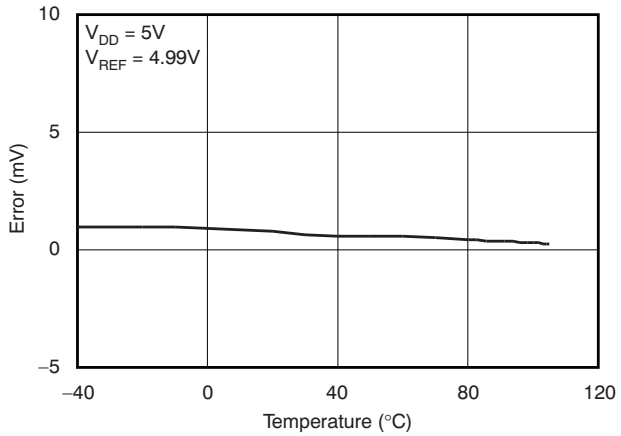


Figure 5. Zero-Scale Error vs Temperature

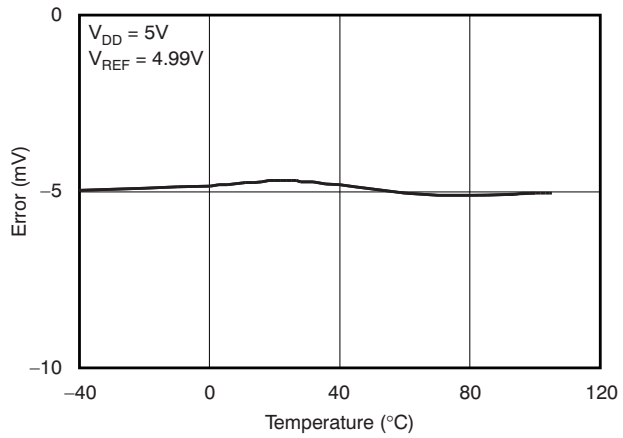


Figure 6. Full-Scale Error vs Temperature

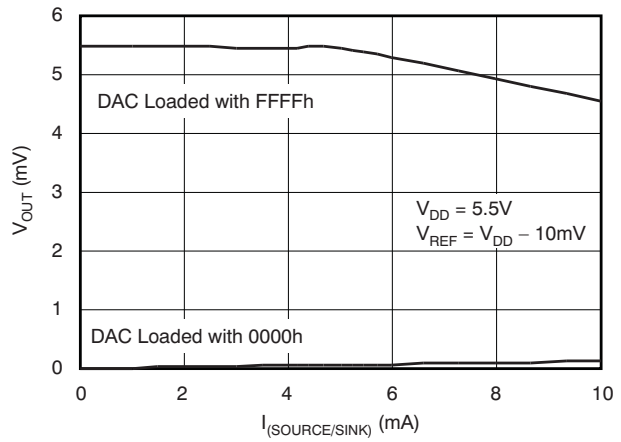


Figure 7. Source and Sink Current Capability

V_{DD} = 5 V (continued)

At T_A = 25°C (unless otherwise noted)

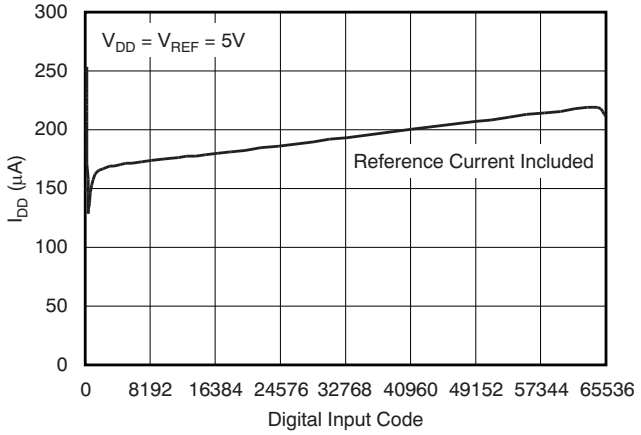


Figure 8. Supply Current vs Digital Input Code

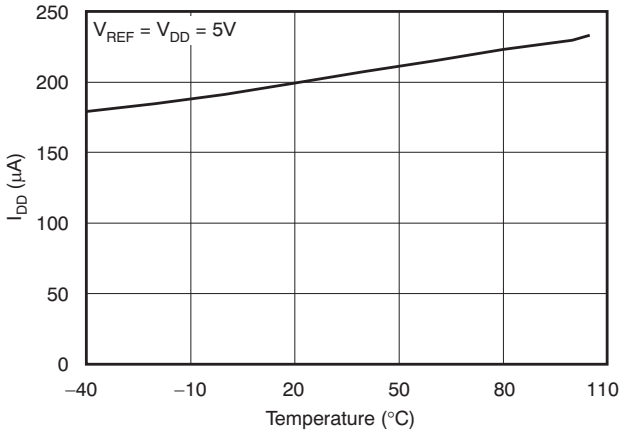


Figure 9. Power-Supply Current vs Temperature

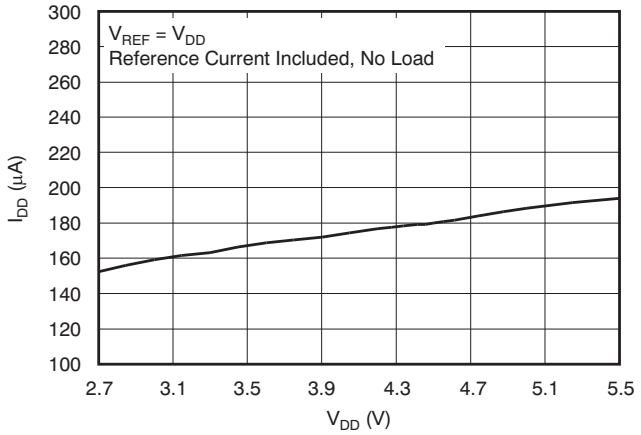


Figure 10. Supply Current vs Supply Voltage

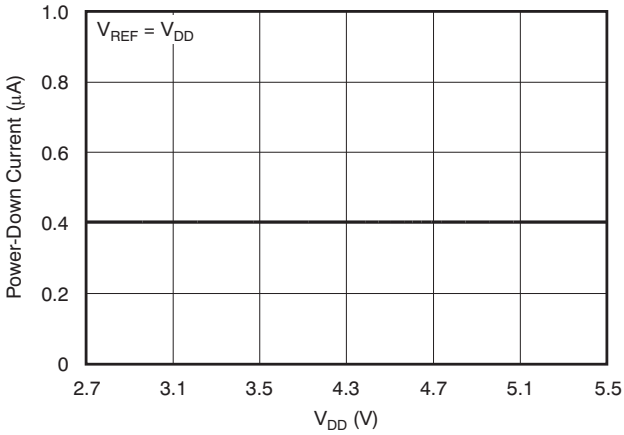


Figure 11. Power-Down Current vs Supply Voltage

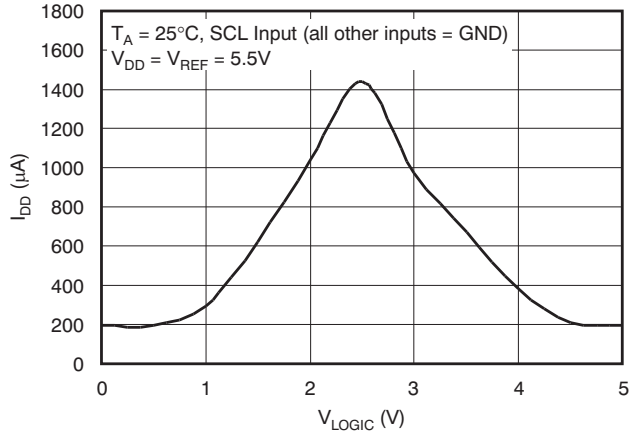


Figure 12. Supply Current vs Logic Input Voltage

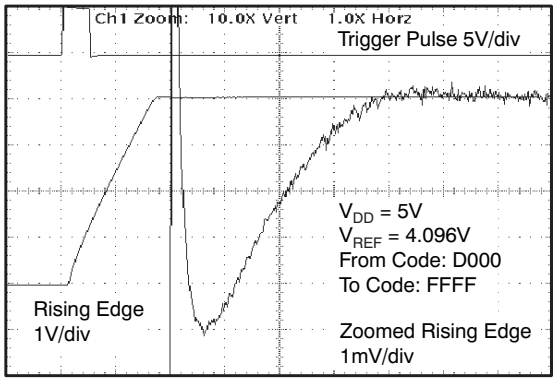


Figure 13. Full-Scale Settling Time, 5-V Rising Edge

V_{DD} = 5 V (continued)

At T_A = 25°C (unless otherwise noted)

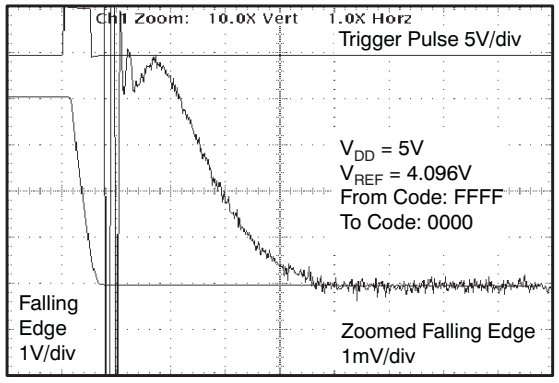


Figure 14. Full-Scale Settling Time, 5-V Falling Edge

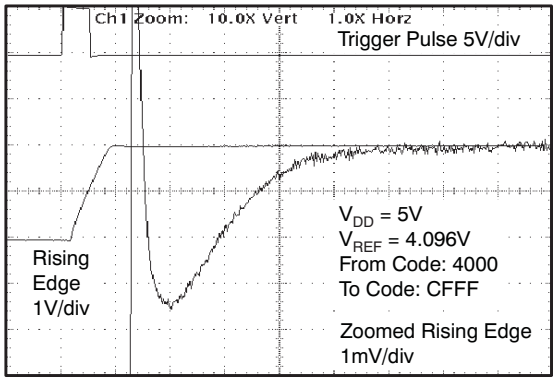


Figure 15. Half-Scale Settling Time, 5-V Rising Edge

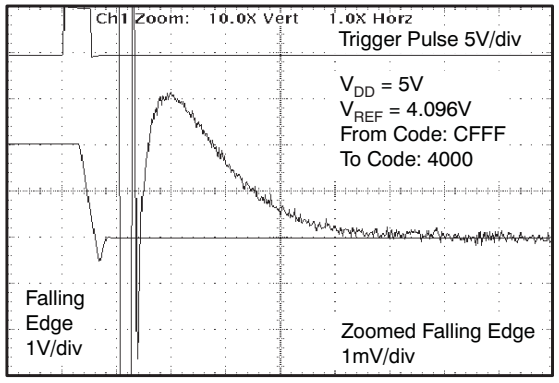


Figure 16. Half-Scale Settling Time, 5-V Falling Edge

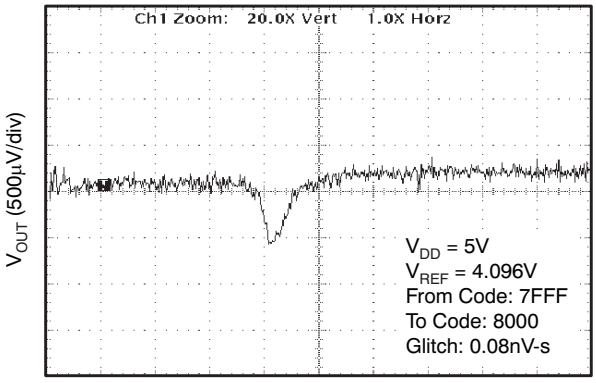


Figure 17. Glitch Energy: 5-V, 1-LSB Step, Rising Edge

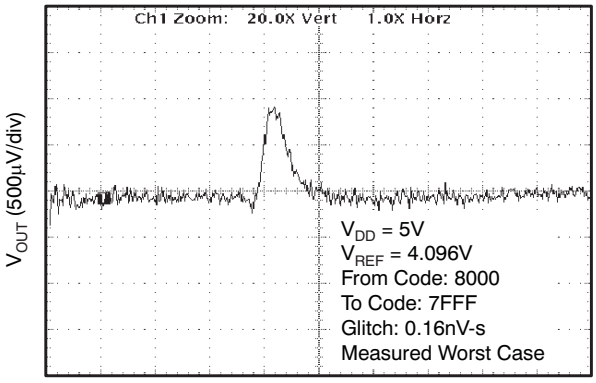


Figure 18. Glitch Energy: 5-V, 1-LSB Step, Falling Edge

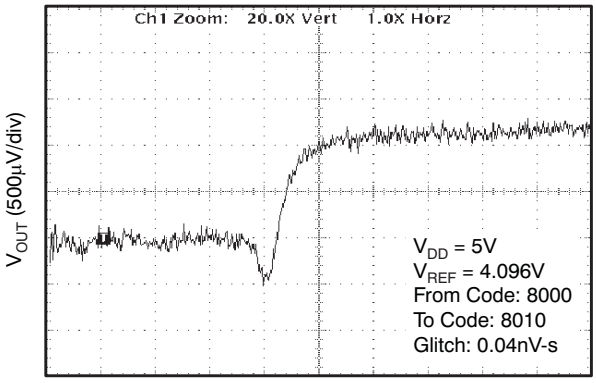


Figure 19. Glitch Energy: 5-V, 16-LSB Step, Rising Edge

V_{DD} = 5 V (continued)

At T_A = 25°C (unless otherwise noted)

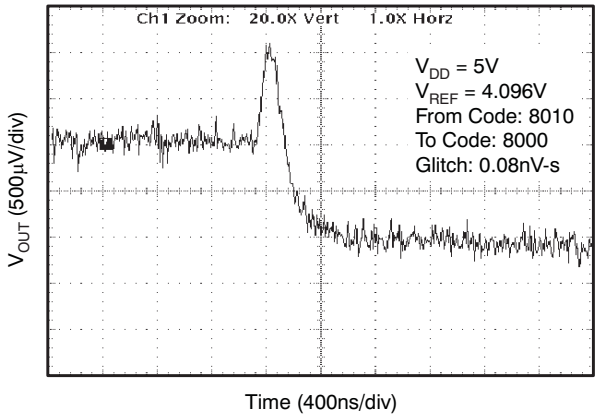


Figure 20. Glitch Energy: 5-V, 16-LSB Step, Falling Edge

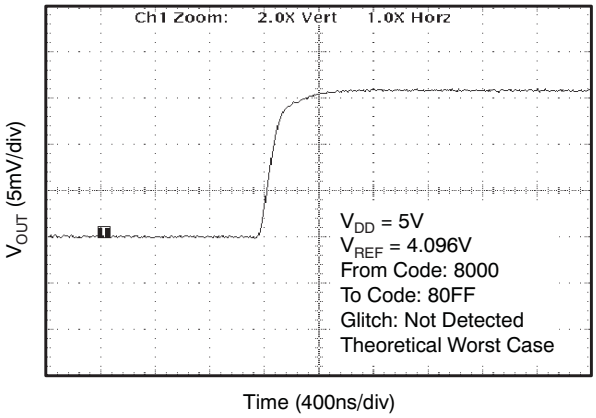


Figure 21. Glitch Energy: 5-V, 256-LSB Step, Rising Edge

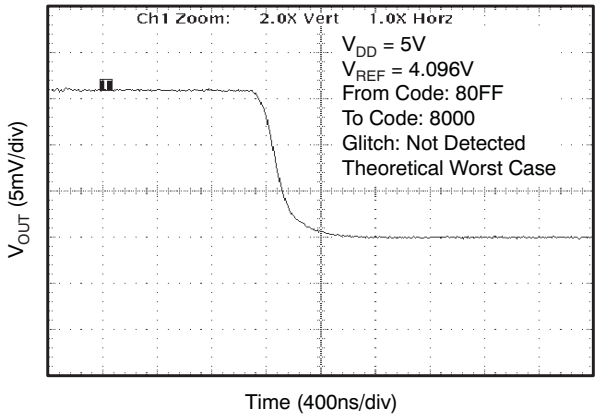


Figure 22. Glitch Energy: 5-V, 256-LSB Step, Falling Edge

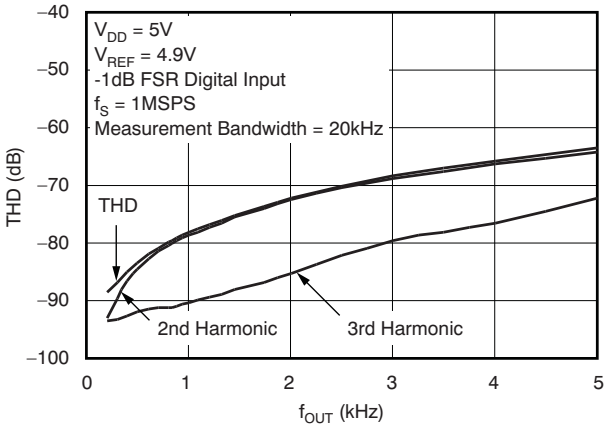


Figure 23. Total Harmonic Distortion vs Output Frequency

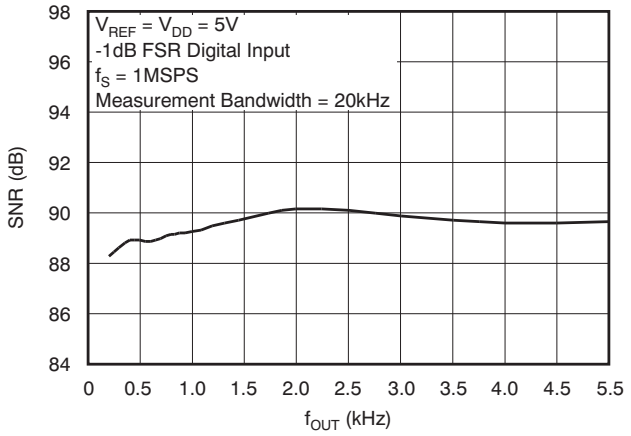


Figure 24. Signal-to-Noise Ratio vs Output Frequency

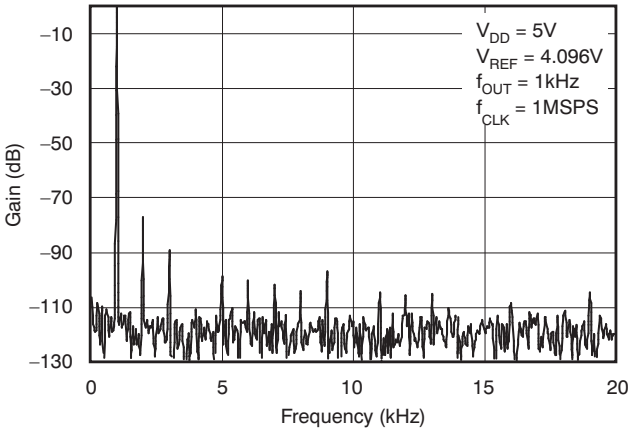


Figure 25. Power Spectral Density

V_{DD} = 5 V (continued)

At T_A = 25°C (unless otherwise noted)

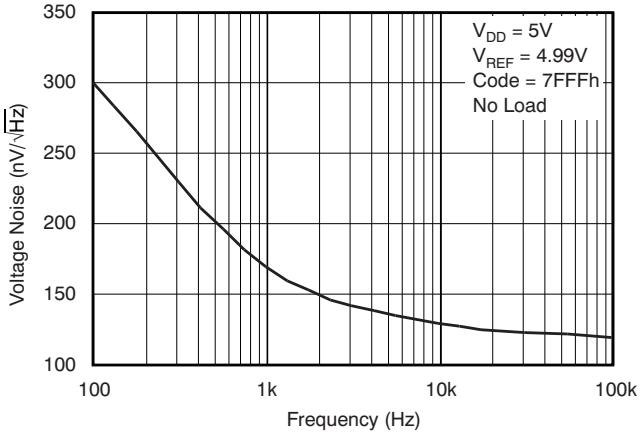


Figure 26. Output Noise Density

6.7.2 V_{DD} = 2.7 V

At T_A = 25°C (unless otherwise noted)

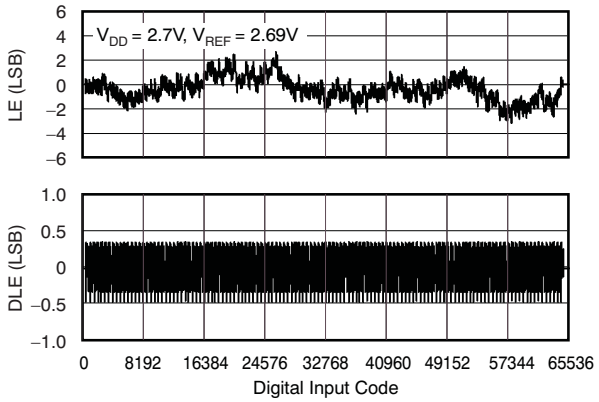


Figure 27. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

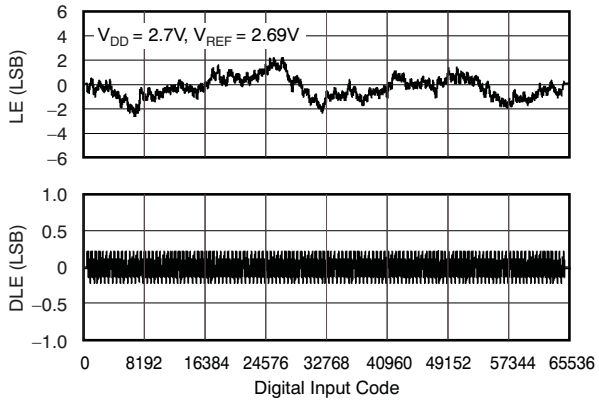


Figure 28. Linearity Error and differential Linearity Error vs Digital Input Code

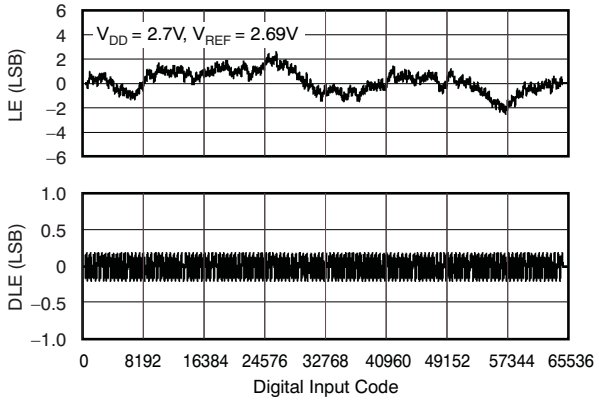


Figure 29. Linearity Error and Differential Linearity Error vs Digital Input Code (105°C)

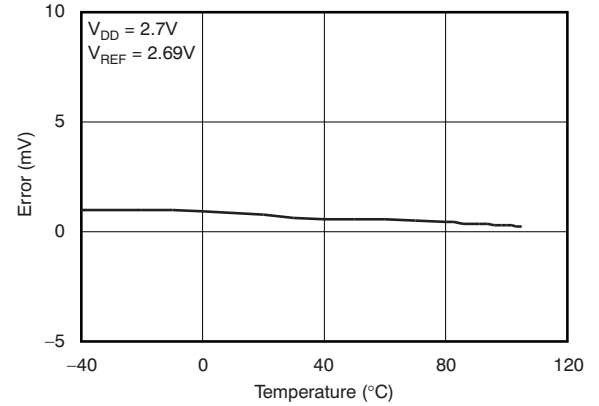


Figure 30. Zero-Scale Error vs Temperature

V_{DD} = 2.7 V (continued)

At T_A = 25°C (unless otherwise noted)

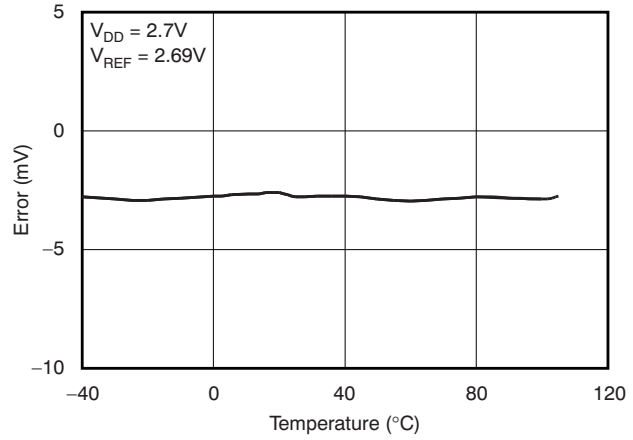


Figure 31. Full-Scale Error vs Temperature

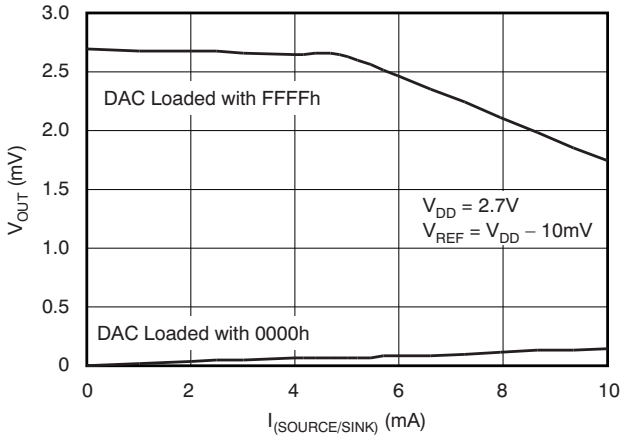


Figure 32. Source and Sink Current Capability

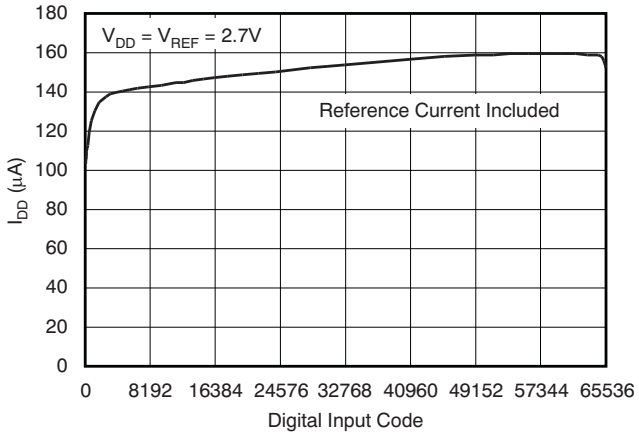


Figure 33. Supply Current vs Digital Input Code

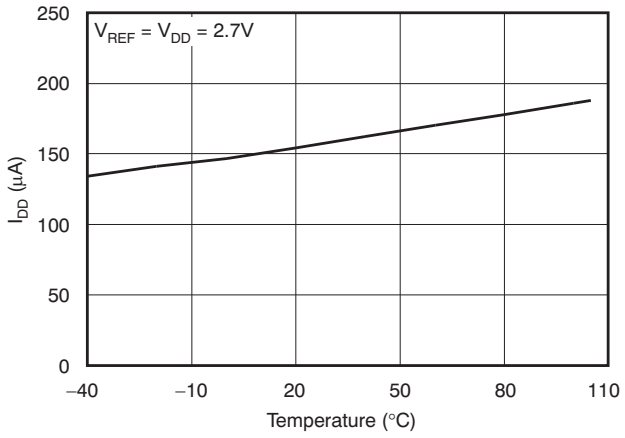


Figure 34. Power-Supply Current vs Temperature

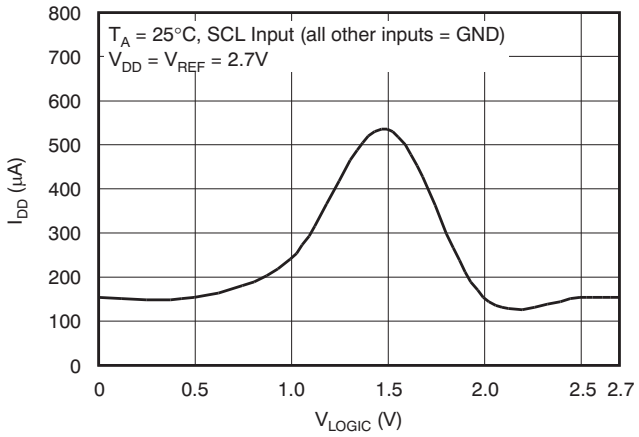


Figure 35. Supply Current vs Logic Input Voltage

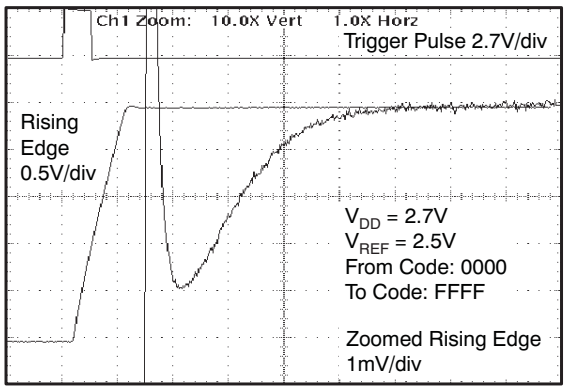


Figure 36. Full-Scale Settling Time: 2.7-V Rising Edge

V_{DD} = 2.7 V (continued)

At T_A = 25°C (unless otherwise noted)

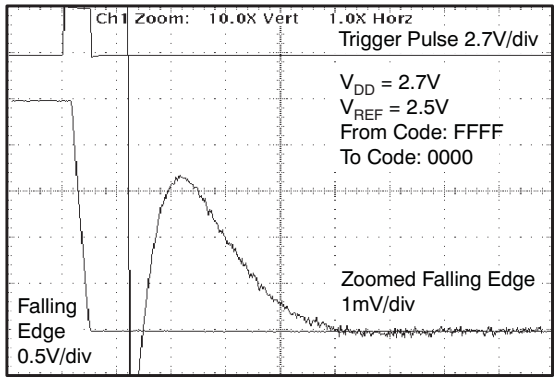


Figure 37. Full-Scale Settling Time: 2.7-V Falling Edge

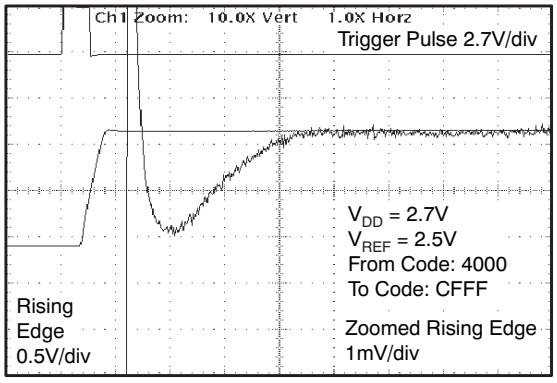


Figure 38. Half-Scale Settling Time: 2.7-V Rising Edge

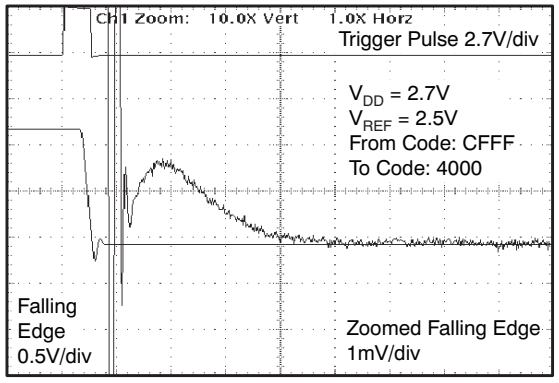


Figure 39. Half-Scale Settling Time: 2.7-V Falling Edge

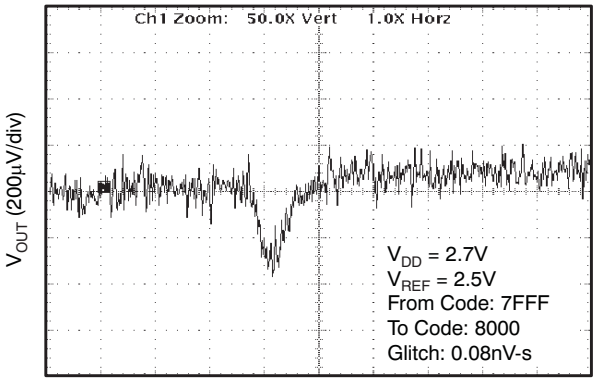


Figure 40. Glitch Energy: 2.7-V, 1-LSB Step, Rising Edge

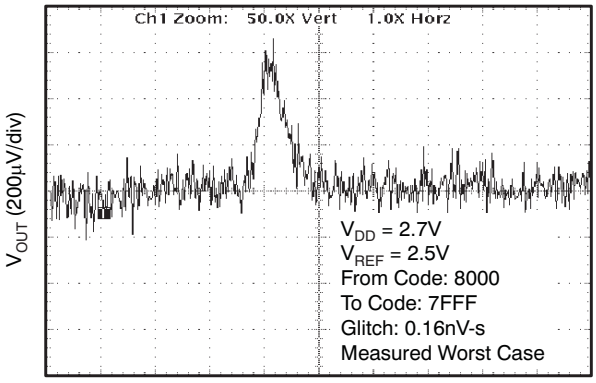


Figure 41. Glitch Energy: 2.7-V, 1-LSB Step, Falling Edge

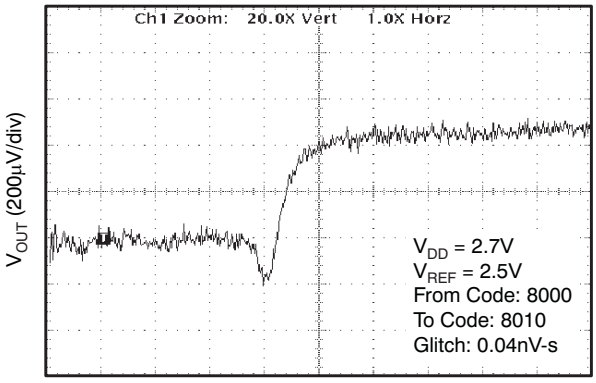


Figure 42. Glitch Energy: 2.7-V, 16-LSB Step, Rising Edge

V_{DD} = 2.7 V (continued)

At T_A = 25°C (unless otherwise noted)

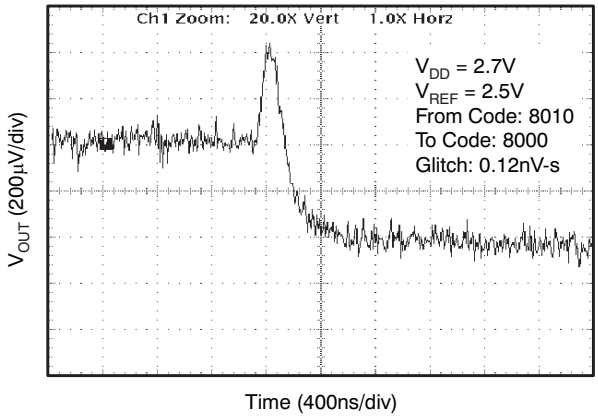


Figure 43. Glitch Energy: 2.7-V, 16-LSB Step, Falling Edge

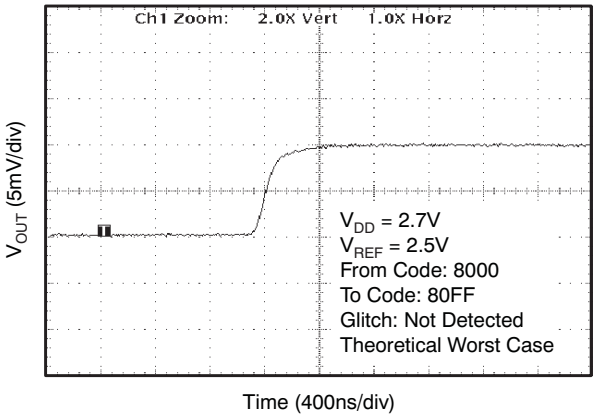


Figure 44. Glitch Energy: 2.7-V, 256-LSB Step, Rising Edge

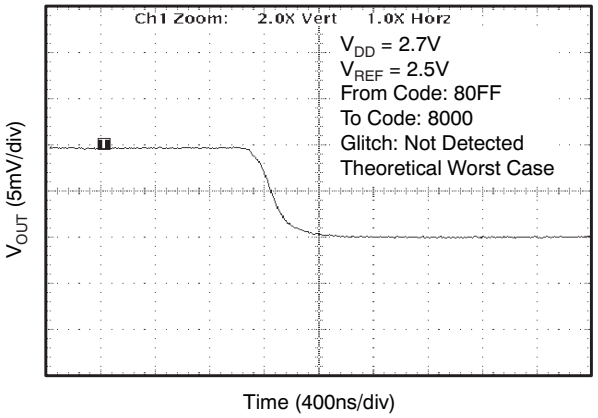


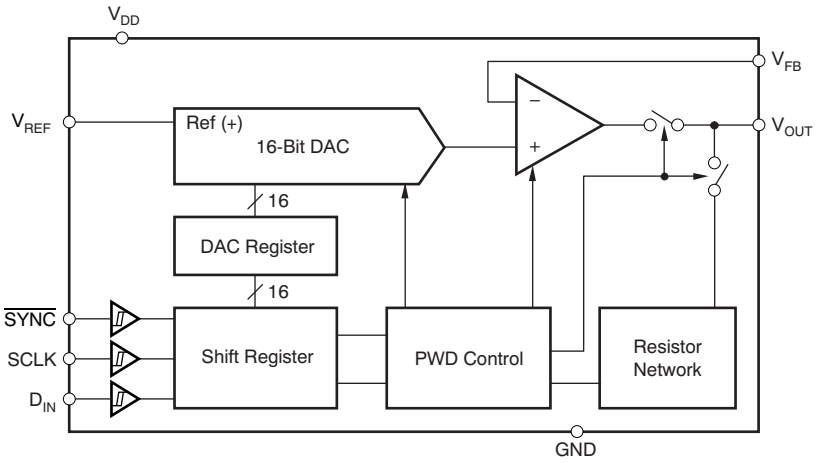
Figure 45. Glitch Energy: 2.7-V, 256-LSB Step, Falling Edge

7 Detailed Description

7.1 Overview

The DAC8551 is a small, low-power, voltage output, single-channel, 16-bit, DAC. The device is monotonic by design, provides excellent linearity, and minimizes undesired code-to-code transient voltages. The DAC8551 uses a versatile, three-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DAC Section

The DAC8551 architecture consists of a string DAC followed by an output buffer amplifier. Figure 46 shows a block diagram of the DAC architecture.

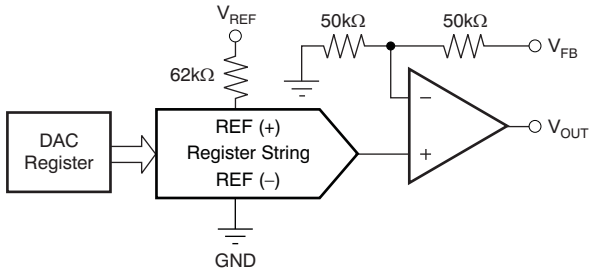


Figure 46. DAC8551 Architecture

The input coding to the DAC8551 is straight binary, so the ideal output voltage is given by:

$$V_O = \frac{D_{IN}}{65536} \times V_{REF}$$

where

- D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535 (1)

7.3.1.1 Resistor String

The resistor string section is shown in Figure 47. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured because of the string resistor architecture.

Feature Description (continued)

7.3.1.2 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the *Typical Characteristics* section *V_{DD} = 5 V*. The slew rate is 1.8 V/µs with a full-scale setting time of 8 µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This configuration allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

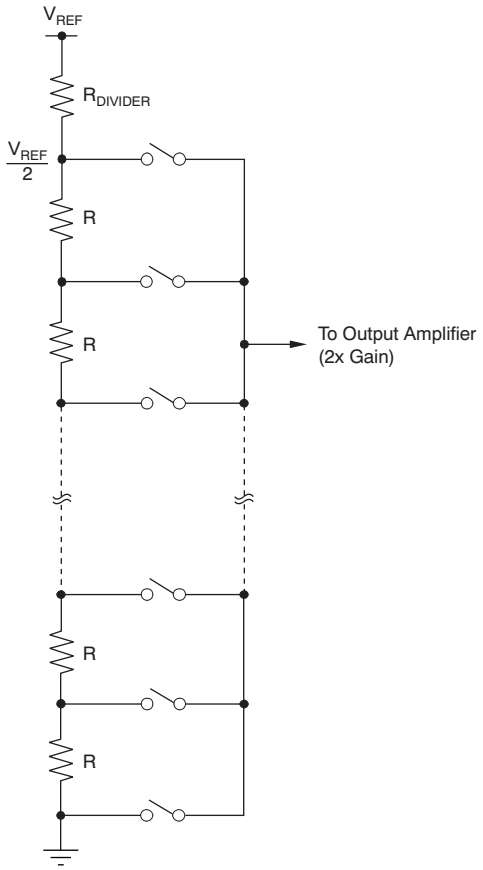


Figure 47. Resistor String

7.3.2 Power-On Reset

The DAC8551 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0 V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

7.4 Device Functional Modes

7.4.1 Power-Down Modes

The DAC8551 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1 shows how the state of the bits corresponds to the mode of operation of the device.

Table 1. Operating Modes

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
Power-down modes		
0	1	Output typically 1 kΩ to GND
1	0	Output typically 100 kΩ to GND
1	1	High-Z

When both bits are set to '0', the device works normally with its typical current consumption of 200 µA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options. The output is connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 48.

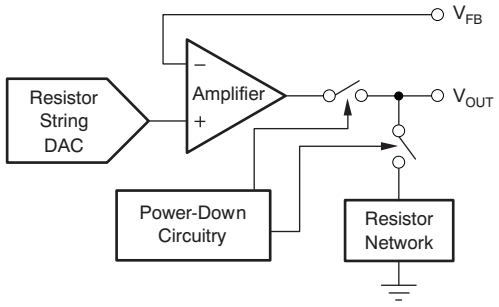


Figure 48. Output Stage During Power-Down

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V, and 5 µs for V_{DD} = 3 V. See *Typical Characteristics* for more information.

7.5 Programming

7.5.1 Serial Interface

The DAC8551 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See Figure 1 for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the DAC8551 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. As previously mentioned, it must be brought HIGH again just before the next write sequence.

Programming (continued)

7.5.2 Input Shift Register

The input shift register is 24 bits wide, as shown in Figure 49. The first six bits are *unused* bits. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). A more complete description of the various modes is located in *Power-Down Modes*. The next 16 bits are the data bits. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused						PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 49. DAC8551 Data Input Register Format

7.5.3 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 50.

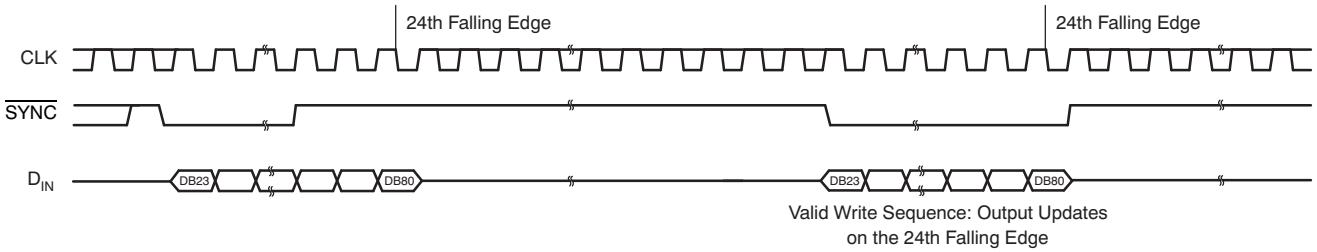


Figure 50. $\overline{\text{SYNC}}$ Interrupt Facility

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low-power consumption of the DAC8551 lends itself to applications such as loop-powered control where the current dissipation of each device is critical. The low power consumption also allows the DAC8551 to be powered using only a precision reference for increased accuracy. The low-power operation coupled with the ultra-low power power-down modes also make the DAC8551 a great choice for battery and portable applications.

8.1.1 Bipolar Operation Using the DAC8551

The DAC8551 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 51. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the operational amplifier. See *CMOS, Rail-to-Rail, I/O Operational Amplifiers* (SBOS180) for more information.

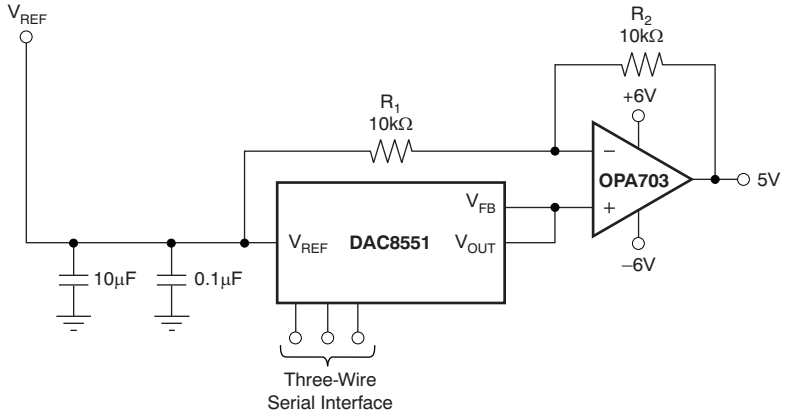


Figure 51. Bipolar Output Range

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_2}{R_1} \right) \right] \quad (2)$$

where

- D is the input code in decimal (0–65535)

With V_{REF} = 5 V, R_1 = R_2 = 10 kΩ.

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5 \text{ V} \quad (3)$$

Using this example, an output voltage range of ±5 V—with 0000h corresponding to a –5-V output and FFFFh corresponding to a 5-V output—can be achieved. Similarly, using V_{REF} = 2.5 V, a ±2.5-V output voltage range can be achieved.

8.2 Typical Application

8.2.1 Loop-Powered, 2-Wire, 4-mA to 20-mA Transmitter With XTR116

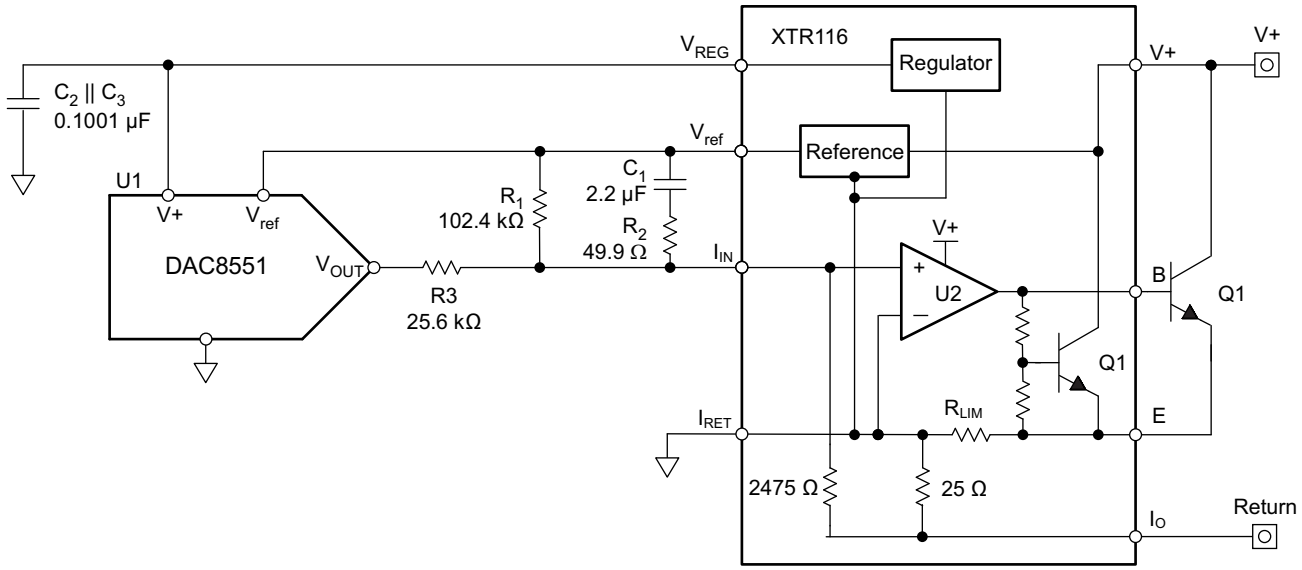


Figure 52. Loop-Powered Transmitter

8.2.1.1 Design Requirements

This design is commonly referred to as a loop-powered, or 2-wire, 4-mA to 20-mA transmitter. The transmitter has only two external input terminals: a supply connection and an output, or return, connection. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of its return current. In order to conform to the 4-mA to 20-mA communication standard, the complete transmitter must consume less than 4 mA of current. The DAC8551 enables the accurate control of the loop current from 4 mA to 20 mA in 16-bit steps.

8.2.1.2 Detailed Design Procedure

Although it is possible to recreate the loop-powered circuit using discrete components, the XTR116 provides simplicity and improved performance due to the matched internal resistors. The output current can be modified if necessary by looking using Equation 4.

$$I_{OUT}(Code) = \left(\frac{V_{ref} \times Code}{2^N \times R_3} + \frac{V_{REG}}{R_1} \right) \times \left(1 + \frac{2475\ \Omega}{25\ \Omega} \right) \quad (4)$$

See *2-wire, 4-mA to 20-mA Transmitter, EMC/EMI Tested Reference Design* (TIDUAO7) for more information. It covers in detail the design of this circuit as well as how to protect it from EMC/EMI tests.

8.2.1.3 Application Curves

Total unadjusted error (TUE) is a good estimate for the performance of the output as shown in Figure 53. The linearity of the output or INL is in Figure 54.

Typical Application (continued)

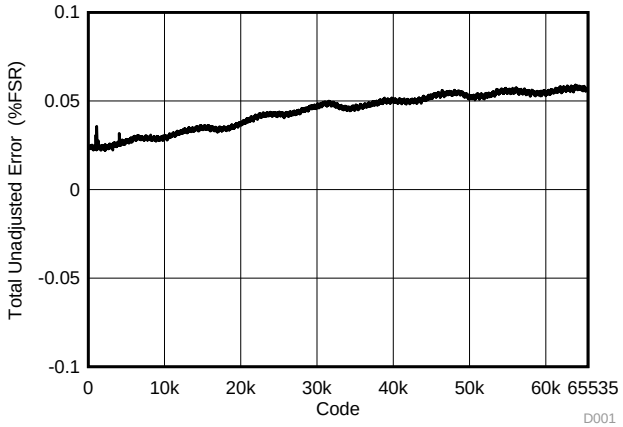


Figure 53. Total Unadjusted Error

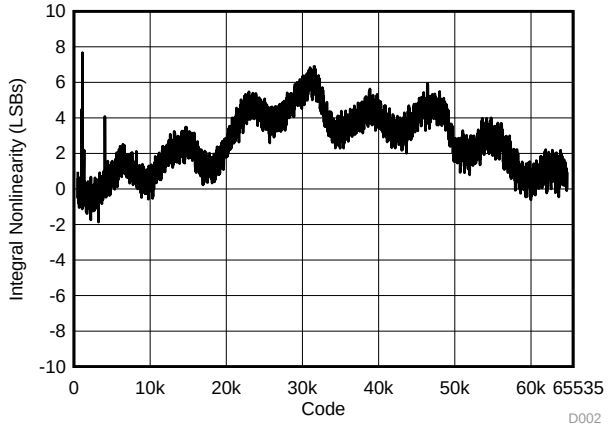


Figure 54. Integral Nonlineareity

8.2.2 Using the REF02 as a Power Supply for the DAC8551

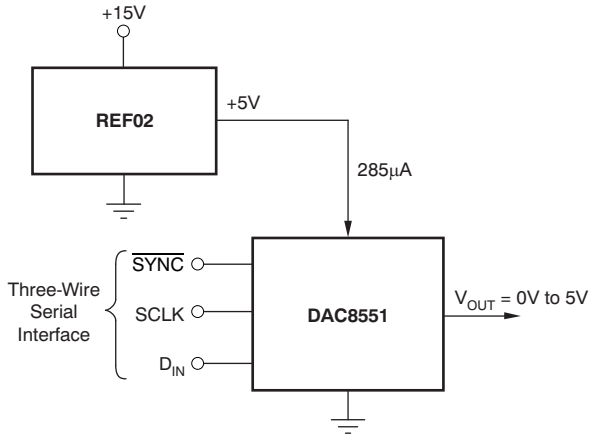


Figure 55. REF02 as a Power Supply to the DAC8551

8.2.2.1 Design Requirements

Due to the extremely low supply current required by the DAC8551, an alternative option is to use the REF02 to supply the required voltage to the device, as illustrated in Figure 55. See *+5V Precision Voltage Reference* (SBVS003) for more inforation.

8.2.2.2 Detailed Design Procedure

This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC8551. If the REF02 is used, the current it needs to supply to the DAC8551 is 200 µA. This configuration is with no load on the output of the DAC. When a DAC output is loaded, the REF02 also needs to supply the current to the load.

The total typical current required (with a 5-kΩ load on the DAC output) is:

$$200\ \mu A + \frac{5\ V}{5\ k\Omega} = 1.2\ mA \quad (5)$$

The load regulation of the REF02 is typically 0.005%/mA, resulting in an error of 299 µV for the 1.2-mA current drawn from it. This value corresponds to a 3.9-LSB error.

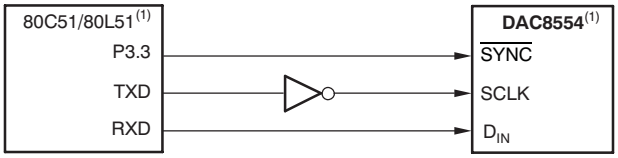
8.3 System Examples

8.3.1 Microprocessor Interfacing

8.3.1.1 DAC8551 to 8051 Interface

Figure 56 shows a serial interface between the DAC8551 and a typical 8051-type microcontroller.

The interface is setup with the TXD of the 8051 drives SCLK of the DAC8551, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the DAC8551, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8551 requires data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

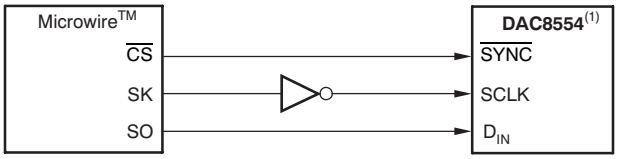


NOTE: (1) Additional pins omitted for clarity.

Figure 56. DAC8551 to 80C51 or 80L51 Interface

8.3.1.2 DAC8551 to Microwire Interface

Figure 57 shows an interface between the DAC8551 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and is clocked into the DAC8551 on the rising edge of the SK signal.

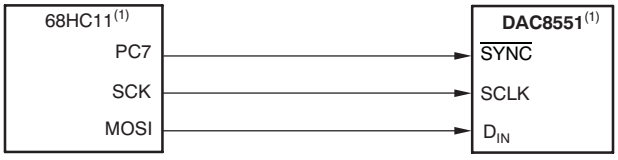


NOTE: (1) Additional pins omitted for clarity.

Figure 57. DAC8551 to Microwire Interface

8.3.1.3 DAC8551 to 68HC11 Interface

Figure 58 shows a serial interface between the DAC8551 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8551, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to the 8051 diagram.



NOTE: (1) Additional pins omitted for clarity.

Figure 58. DAC8551 to 68HC11 Interface

System Examples (continued)

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the $\overline{SYNC}$ line is held LOW (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8551, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken HIGH at the end of this procedure.

9 Power Supply Recommendations

The DAC8551 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to V_{DD} should be well-regulated and low-noise. Switching power supplies and DCDC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. TI recommends including a 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor in order to further minimize noise from the power supply. The current consumption on the V_{DD} pin, the short-circuit current limit, and the load current for the device is listed in *Electrical Characteristics*. The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8551 offers single-supply operation, and it often is used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8551, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

As with the GND connection, V_{DD} should be connected to a 5-V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. TI recommends an additional 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high-frequency noise.

10.2 Layout Example

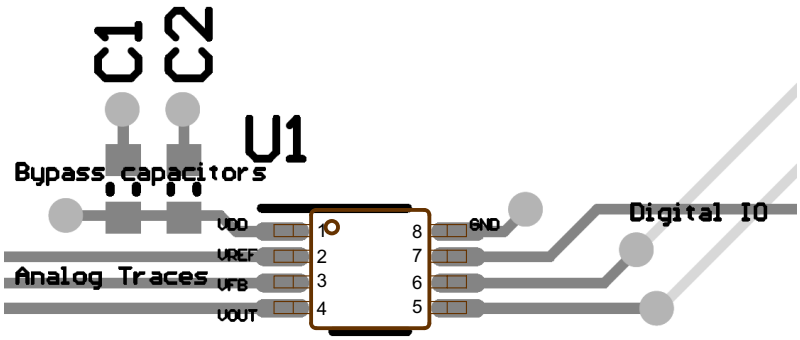


Figure 59. Layout Diagram

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *2-wire, 4-mA to 20-mA Transmitter, EMC/EMI Tested Reference Design*, TIDUAO7
- *+5V Precision Voltage Reference*, SBVS003
- *CMOS, Rail-to-Rail, I/O Operational Amplifiers*, SBOS180

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8551IADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IADGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IADGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	Samples
DAC8551IDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

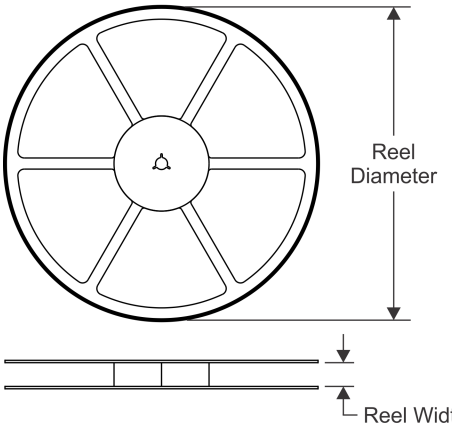
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

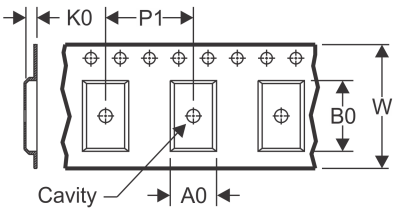
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

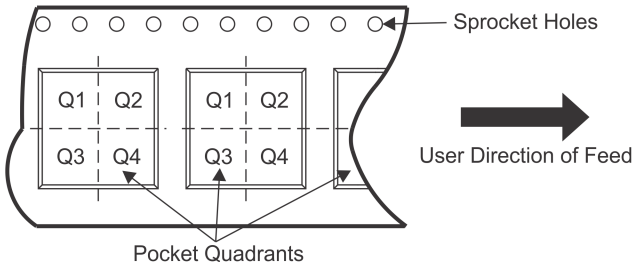


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

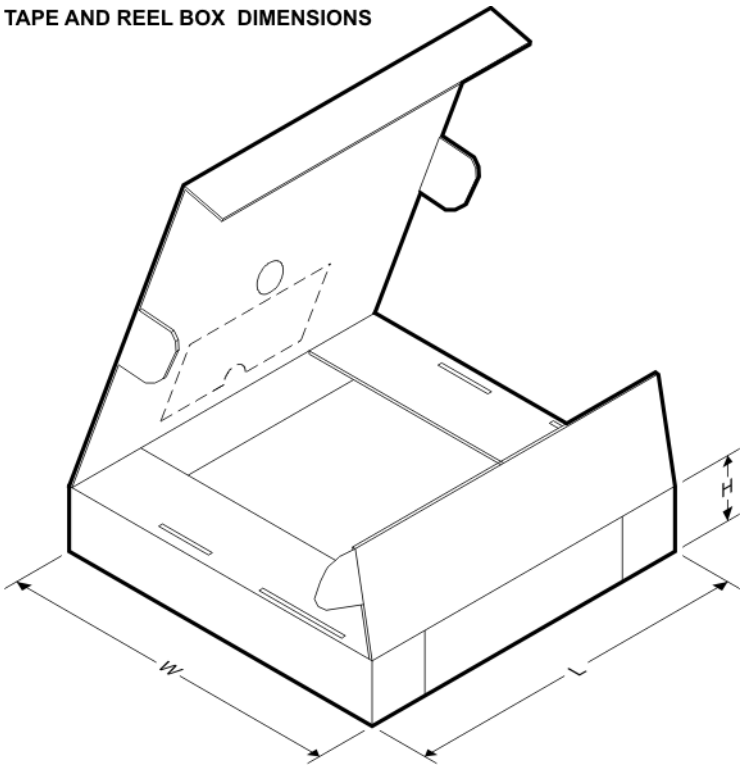
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8551IADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

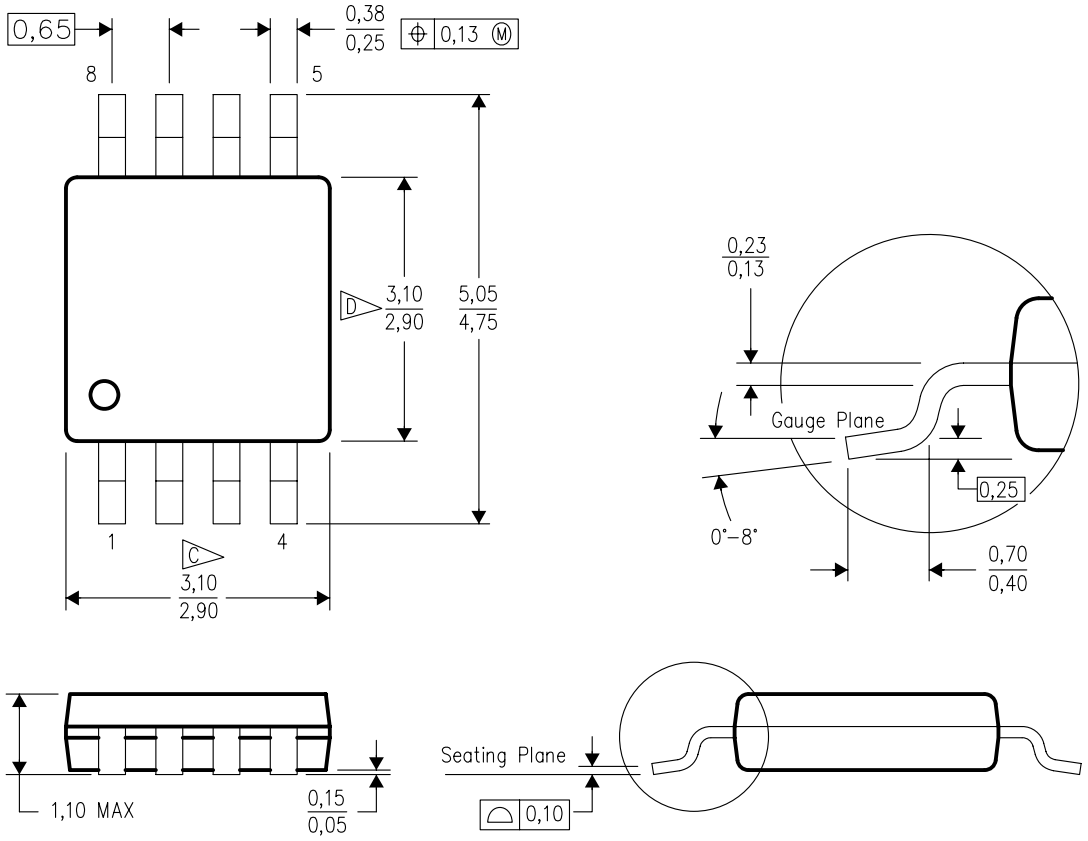
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8551IADGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
DAC8551IADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8551IDGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
DAC8551IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0

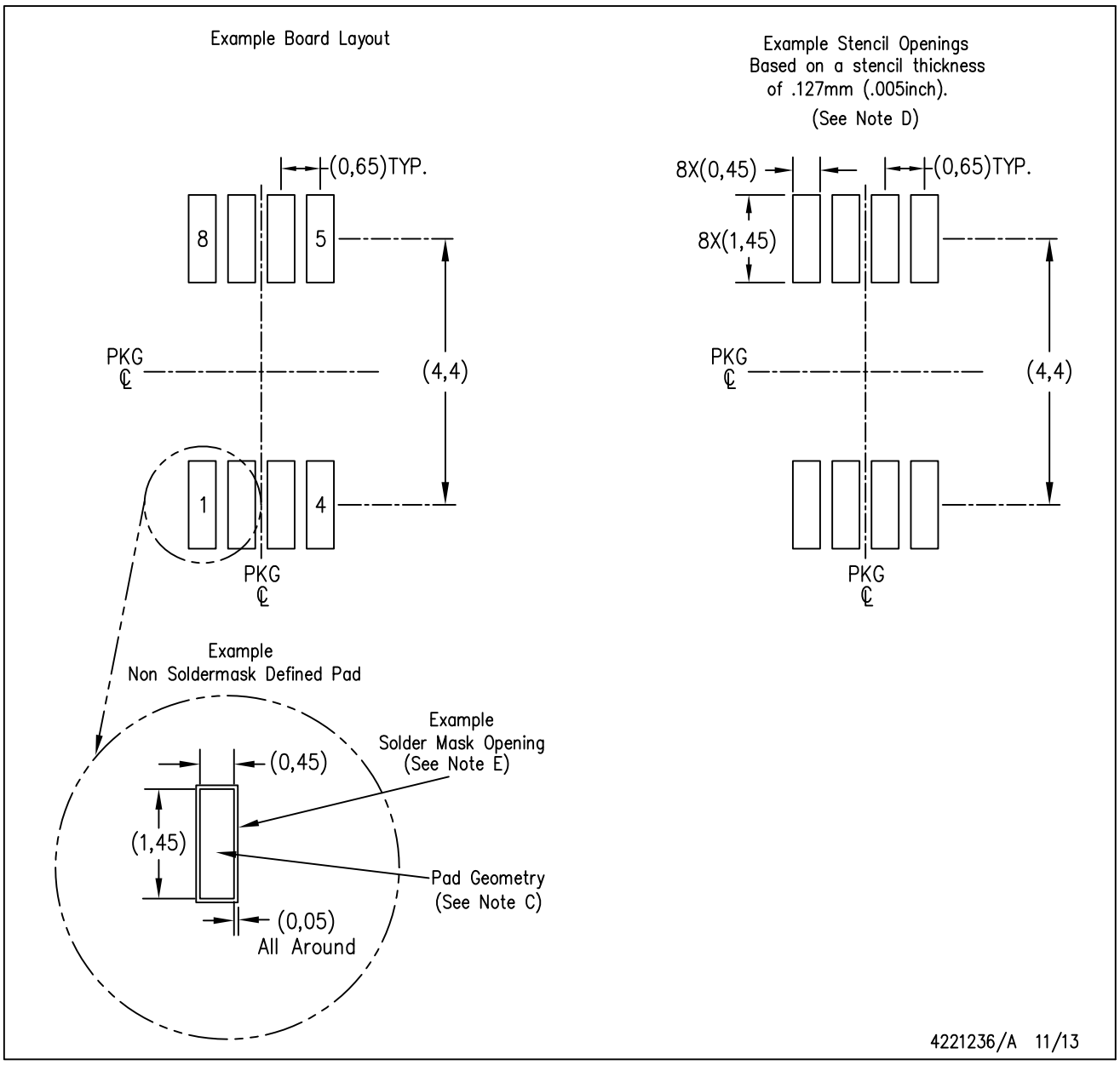
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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