AN994
APPLICATION NOTE

L6384, L6385, L6386 & L6387 APPLICATION GUIDE

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The ST L638X is a versatile high voltage gate driver family.

Realised in BCD Off-line technology, these devices are able to operate with high voltage rails up to 600V. The Gate Drivers provide all the functions and current capability necessary for high side and low side Power MOS and IGBT.

L6384-5-6-7 are High Voltage Drivers for High and Low Side. These devices can be used in all the applications where high voltage shifted control is necessary. These devices have a fairly high driver current capability and they are also provided with an internal patented circuitry which replaces the external bootstrap diode. This feature is achieved by means of a high voltage DMOS, synchronously driven with the low side gate driver.

The **L6384** (Internal diagram in fig. 1) is a half bridge driver with externally adjustable dead-time and shut down function. To disable the driver, the control pin (DT/SD at pin3) must be pulled down below 0.5V. The dead time can be set from 0.5µs to 2.7µs by a simple resistor between pin3 and ground. Available in Minidip and SO8 packages, this driver can be used in motor controls, resonant converters and lighting applications. In fig. 2 the schematic diagram of the evaluation circuit and the layout of the test PCB are shown.

L6384 PIN DESCRIPTION

N.	Name	Type	Function
1	IN(*)	I	Logic Input: it is in phase with HVG and in opposition of phase with LVG. It is compatible to Vcc voltage.
2	V_{CC}	I	Supply input voltage: there is an internal clamp [Typ. 15.6V] There is also an UVLO feature (Typ. Vcc_{th1} = 12V, Vcc_{th2} = 10V).
3	DT/SD	I	High impedence pin with two functionalities. When pulled to a voltage lower than V_{dt} [Typ.0.5V] the device is shut down. A voltage higher than V_{dt} sets the dead time between high side and low side gate driver. The dead time value can be set forcing a certain voltage level on the pin or connecting a resistor between pin 3 and ground. Care must be taken to avoid spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. This pin can not be let floating for the same reason. The pin has not to be pulled through a low impedence to Vcc, because of the drop on the corrent source that feeds Rdt. The operative range is: V_{dt} ... 270K · I_{dt}, that allows a dt range of 0.4 - 3.1µs.
4	GND		Ground
5	LVG	O	Low side driver output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedence also in SD conditions.
6	Vout	O	Upper driver floating reference: layout care has to be taken to avoid undervoltage spikes on this pin

L6384 PIN DESCRIPTION (continued)

N.	Name	Type	Function
7	HVG	O	High side driver output:the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max between this pin and Vout (@I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedence also in SD conditions.
8	V_{boot}		Bootstrap Supply Voltage: it is the upper driver floating supply. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

(*) The pull-down internal resistor is typically some hundreds Kohm.

Figure 1. L6384 Internal Block Diagram.

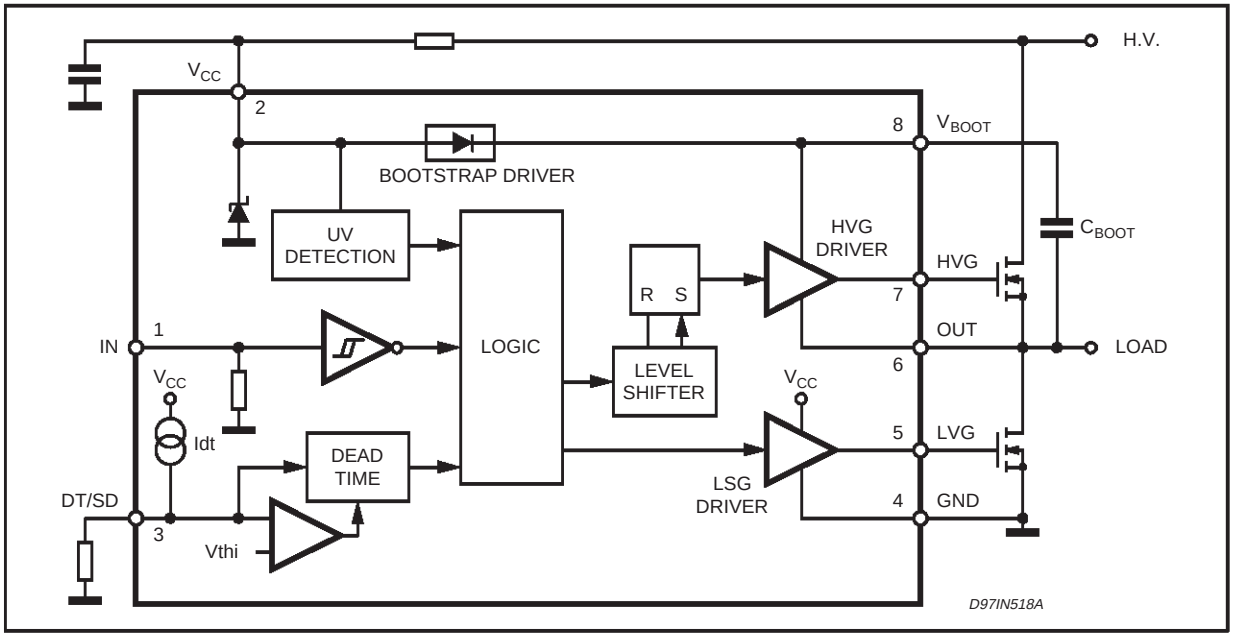


Figure 2. L6384 Schematic diagram of the evaluation circuit.

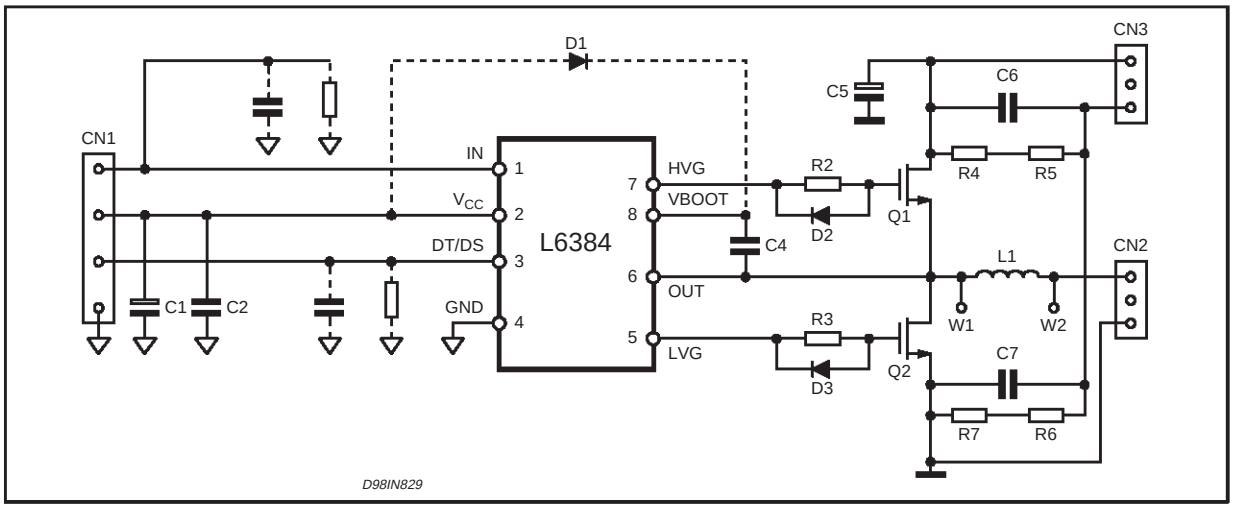
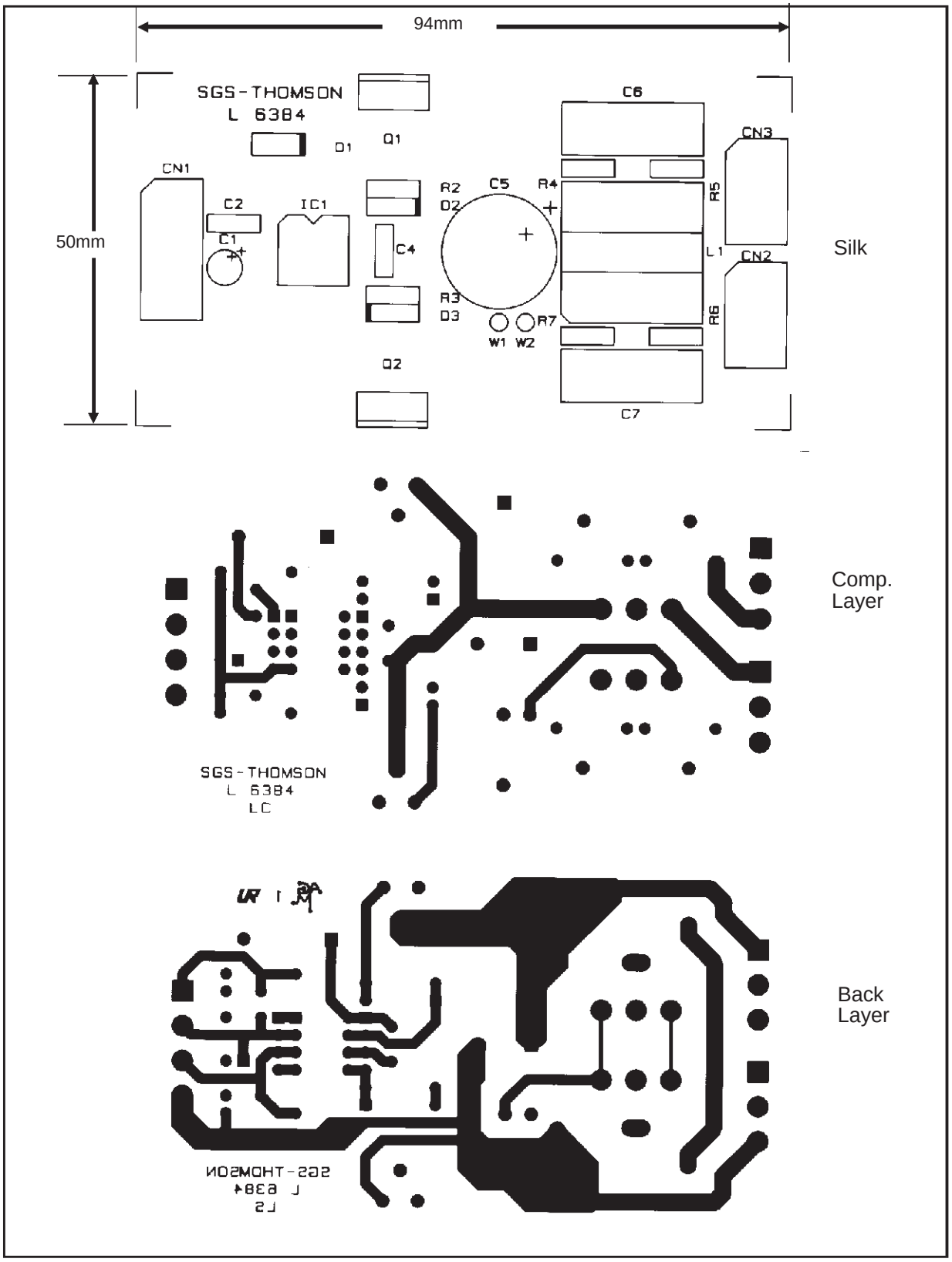


Figure 2a. L6384 - PCB and component layout of the fig. 2.



The **L6385** (Internal diagram in fig. 3) is a high and low side configurable driver. In fact, it is possible to control two separate inputs, thus the outputs can be switched independently. This device is provided with undervoltage detection in both low voltage side and high voltage bootstrapped supply. Delivered in 8pin packages, this driver has been especially designed for power supplies and motion control application. Fig. 4 shows the schematic diagram of the evaluation circuit and the layout of the relevant PCB.

L6385 PIN DESCRIPTION

N.	Name	Type	Function
1	LIN (*)	I	Low Side Driver Logic Input: it is compatible to Vcc voltage. [$V_{il\,Max}$ = 1.5V, $V_{ih\,Min}$ = 3.6V]
2	HIN (*)	I	High Side Driver Logic Input: it is compatible to Vcc voltage. [$V_{il\,Max}$ = 1.5V, $V_{ih\,Min}$ = 3.6V]
3	V_{CC}	I	Supply input voltage with UVLO (Typ. V_{ccth1} = 9.6V, V_{ccth2} = 8.3V).
4	GND		Ground
5	LVG	O	Low Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low.
6	Vout	O	Upper Driver Floating Reference: layout care has to be taken to avoid undervoltage spikes on this pin.
7	HVG	O	High Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max between this pin and V_{out} (@ I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low.
8	Vboot		Bootstrap Supply Voltage:it is the upper driver floating supply [with UVLO: typ. V_{BSth1} = 9.5V, V_{BSth2} = 8.2V]. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

(*) The pull-down internal resistor is typically some hundreds Kohm.

Figure 3. L6385 Internal Block Diagram.

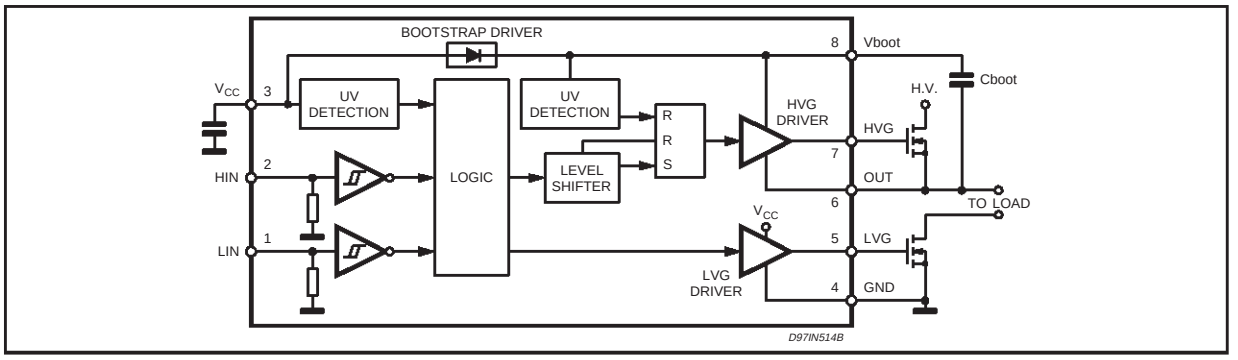


Figure 4. L6385 Schematic diagram of the evaluation circuit.

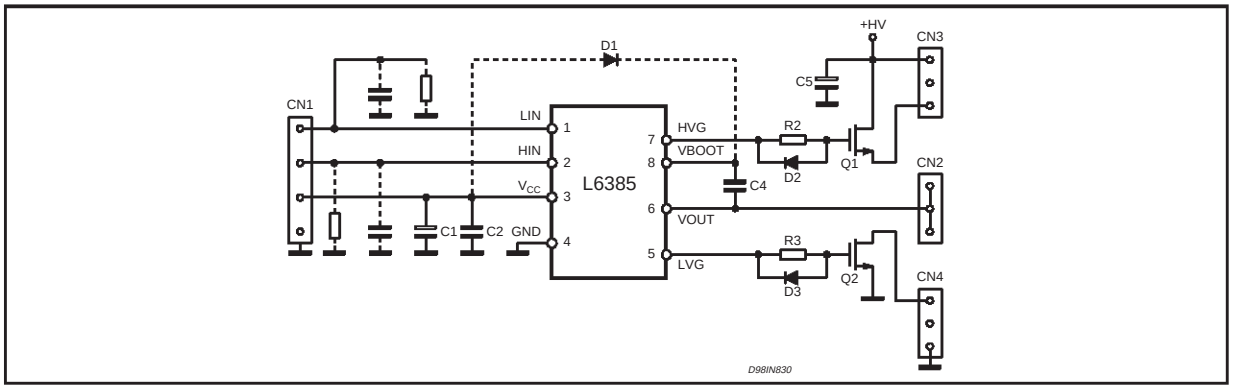
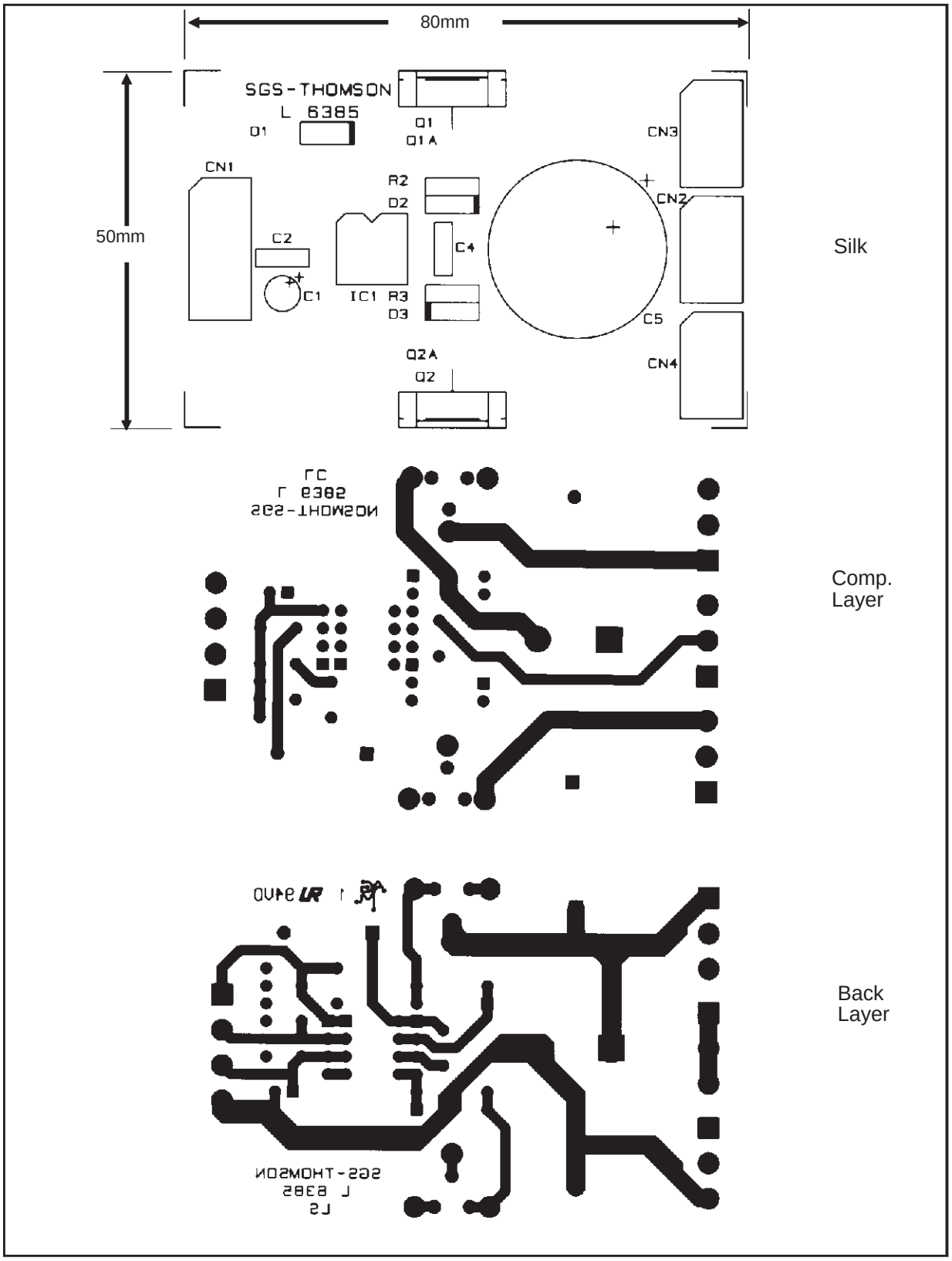


Figure 5a. L6385 - PCB and component layout of the fig. 5.



L6386 (Internal diagram in fig. 5). Configurable driver, the L6386 is based on the L6385 structure with added functions. This device is available in DIP14 or SO14.
The added Shutdown function (active low) and the Current Sense Comparator (0.5V threshold) with Diagnostic Output, make this device particularly suitable for motion control with cycle-by-cycle current feedback. DIAG and CIN pins can be used to stop the device (e.g. acting on SD pin). Fig. 6 shows the schematic diagram of the evaluation circuit and the layout of the relevant PCB.

L6386 PIN DESCRIPTION

N.	Name	Type	Function
1	LIN (*)	I	Lower Driver Logic Input: it is compatible to Vcc voltage. [$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
2	SD (*)	I	Shut Down Logic Input: it is compatible to Vcc voltage. If it has to be pulled up the suggested resistor value is 5-10Kohm. [$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
3	HIN (*)	I	Low Side Driver Logic Input: it is compatible to V_{CC} voltage. [$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
4	V_{CC}	I	Low Side Driver Logic Input: it is compatible to Vcc voltage.[$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
5	DIAG	O	Diagnostic Output: Open Drain
6	CIN	I	Comparator Input
7	SGND		Ground reference for logic signals
8	PGND		Power Ground reference for the Low Voltage Gate Driver
9	LVG	O	Low Side Driver Output: Low side driver output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@ I_{sink} = 10mA) with V_{CC} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedence also in SD conditions.
10, 11	N.C.		Not Connected
12	V_{out}	O	Upper Driver Floating Driver: layout care has to be taken to avoid undervoltage spikes on this pin
13	HVG	O	High Side Driver Output: High side driver output:the output stage can deliver 400mA ource and 650mA sink [Typ. Values] The circuit guarantees 0.3V max between this pin and Vout (@ I_{sink} = 10mA) with V_{CC} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedence also in SD conditions.
14	Vboot		Bootstrapped Supply Voltage: Bootstrap supply voltage: it is the upper driver floating supply [with UVLO: Typ. V_{Bth1} = 11.9V, V_{Bth2} = 9.9V]. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

(*) The pull-down internal resistor is typically some hundreds Kohm.

Figure 5. L6386 Internal Block Diagram.

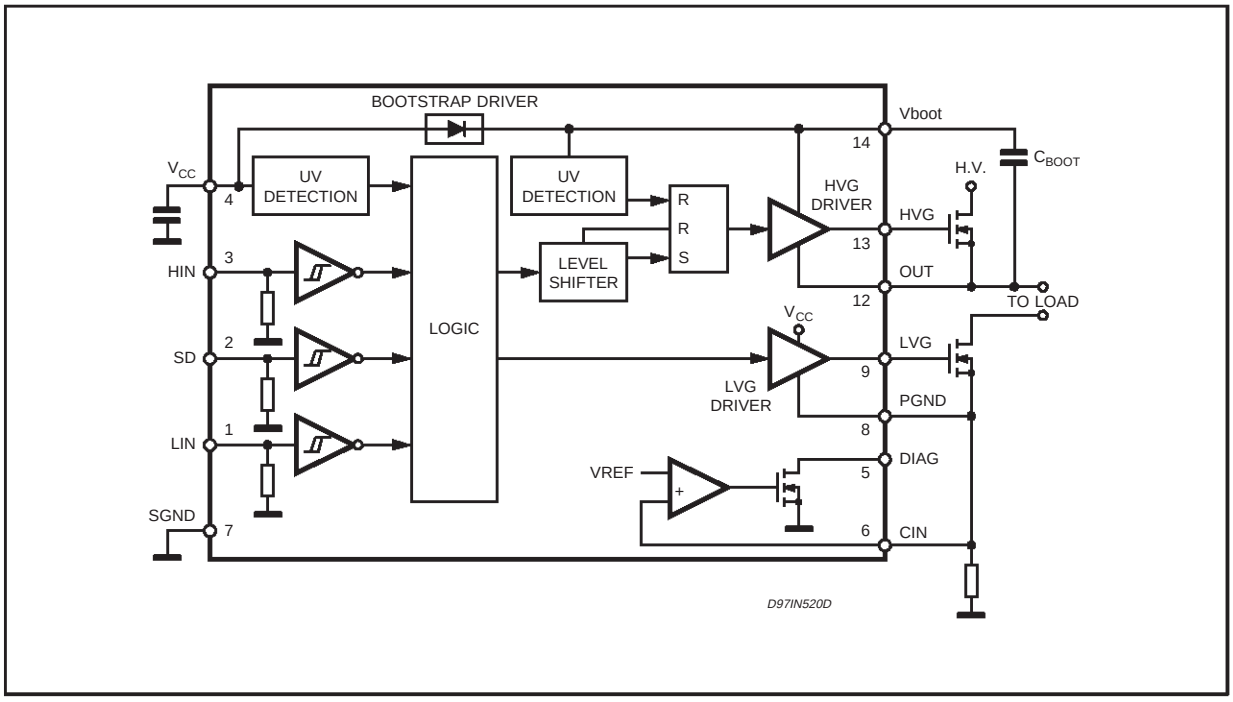


Figure 6. L6386 Schematic diagram of the evaluation circuit.

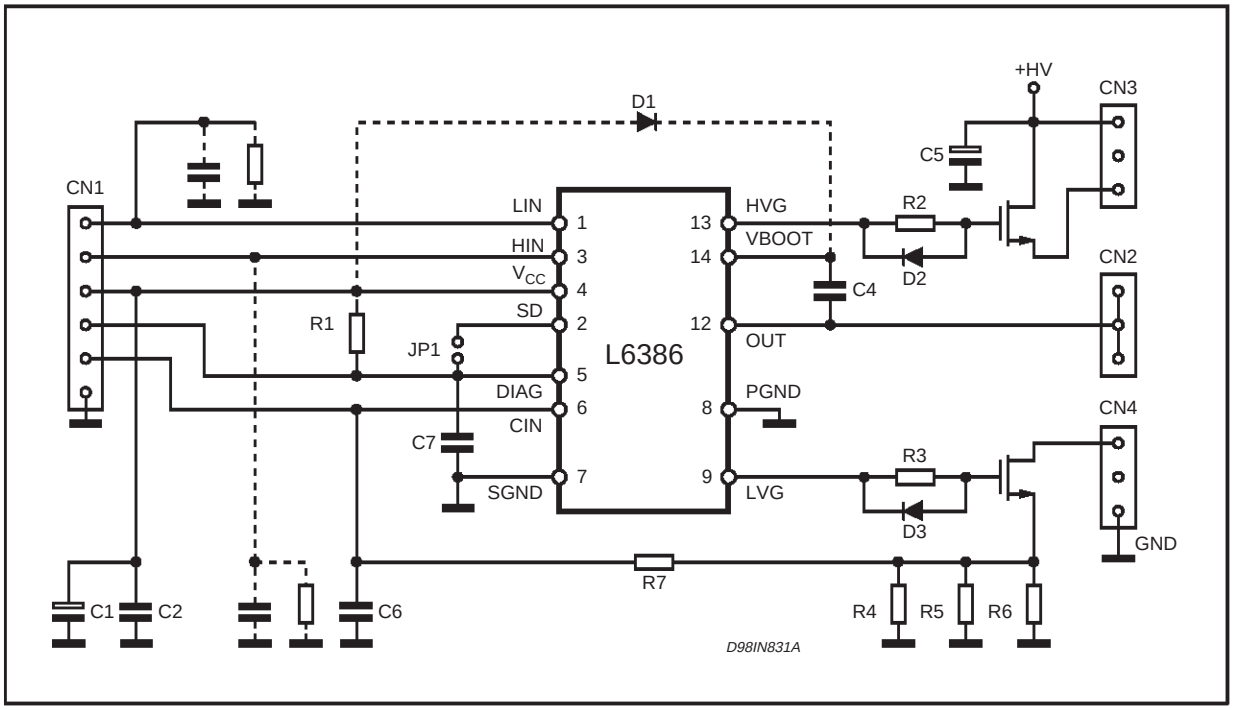
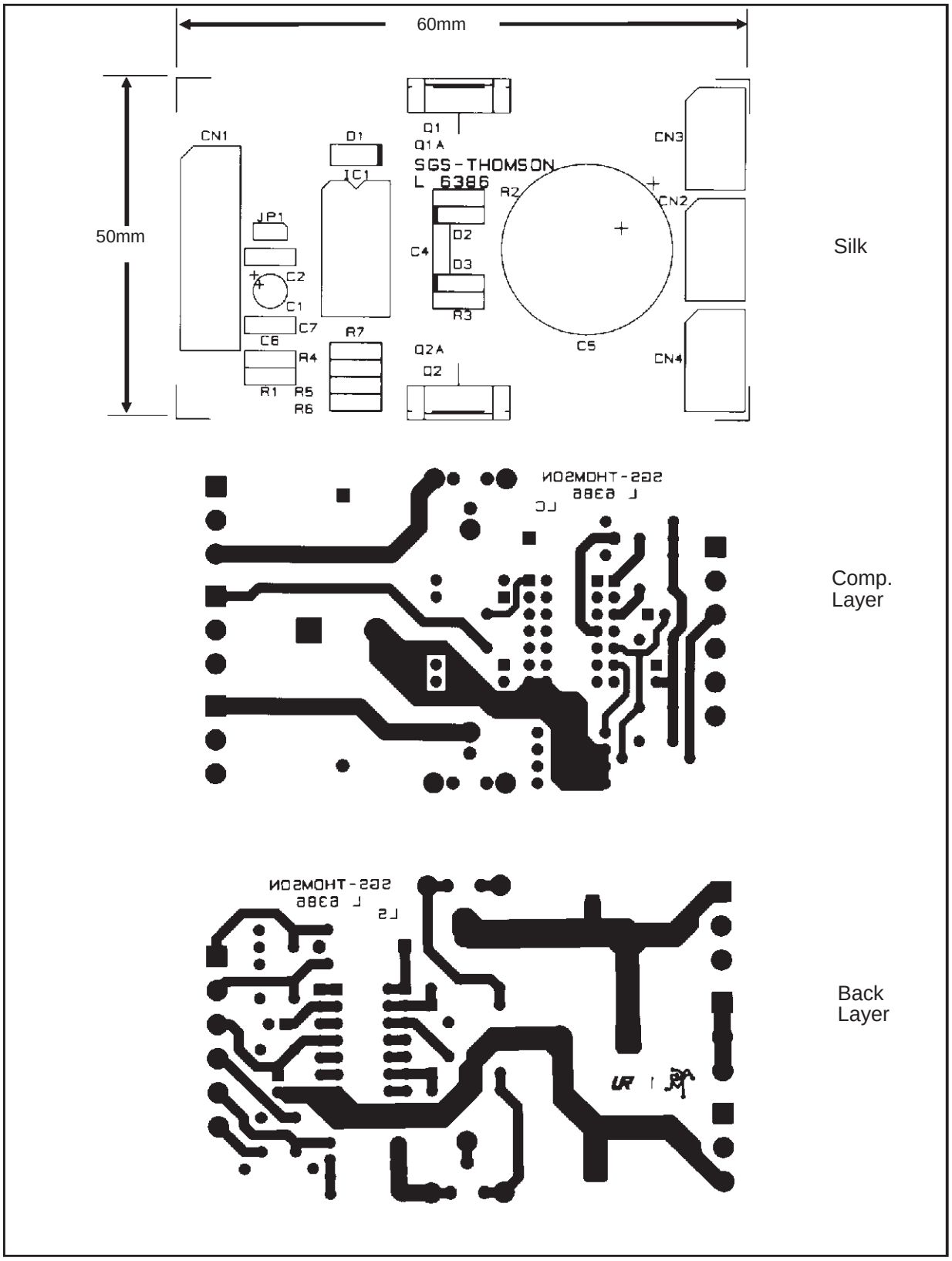


Figure 6a. L6386 - PCB and component layout of the fig. 6.



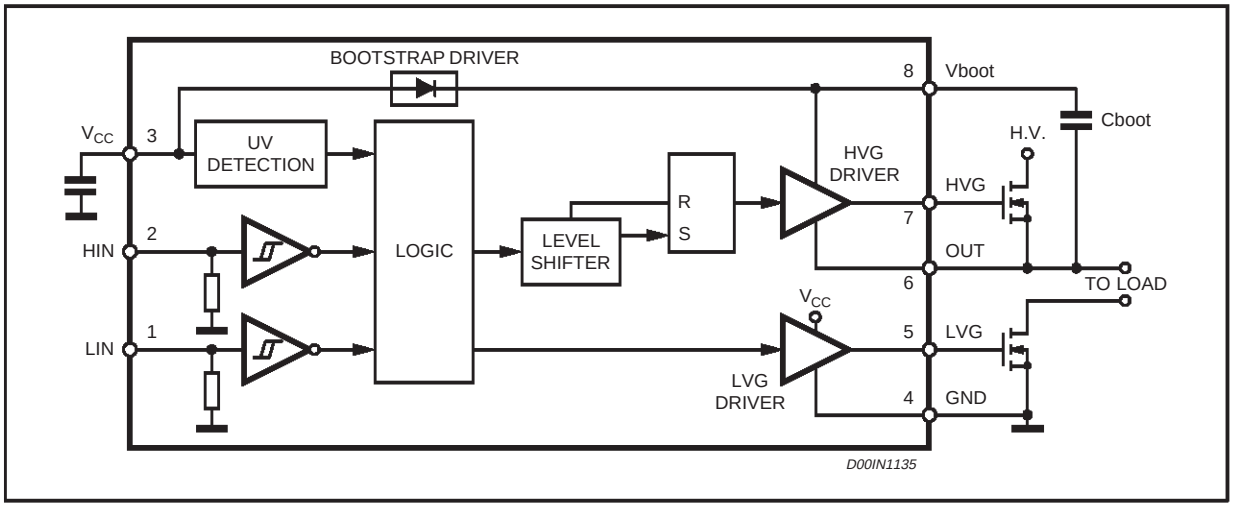
L6387 (internal diagram fig.7) is based on L6385 structure. It has two separate inputs, but there is also an interlocking function to avoid undesired simultaneous turn on of both Power Switches (see Truth Table). The Vcc turn on and turn off thresholds have been lowered to 6V and 5.5V(Typ.). There is no UVLO on the upper driving section.

L6387 PIN DESCRIPTION

N.	Name	Type	Function
1	LIN (*)	I	Low Side Driver Logic Input: it is compatible to Vcc voltage. [$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
2	HIN (*)	I	High Side Driver Logic Input: it is compatible to Vcc voltage. [$V_{il\ Max}$ = 1.5V, $V_{ih\ Min}$ = 3.6V]
3	V_{CC}	I	Supply input voltage [with very low UVLO: V_{ccth1} = 6V & V_{ccth2} = 5.5V (typ.).
4	GND		Ground
5	LVG	O	Low Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low.
6	Vout	O	Upper Driver Floating Reference: layout care has to be taken to avoid undervoltage spikes on this pin.
7	HVG	O	High Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max between this pin and V_{out} (@ I_{sink} = 10mA) with V_{cc} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the the source of the external mosfet normally used to hold the pin low.
8	Vboot		Bootstrap Supply Voltage:it is the upper driver floating supply . The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

(*) The pull-down internal resistor is typically some hundreds Kohm.

Figure 7. L6387 Internal Block Diagram.



L6387: TRUTH TABLE

INPUT	HIN	0	0	1	1
	LIN	0	1	0	1
OUTPUT	HVG	0	0	1	0
	LVG	0	1	0	0

BOOTSTRAP DRIVER

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (fig. 8a). In the L6384-5-6-7 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 8b

An internal charge pump (fig. 8b) provides the DMOS driving voltage .

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

C_{BOOT} selection and charging:

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge :

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss .

It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30nC and V_{gate} is 10V, C_{EXT} is 3nF. With C_{BOOT} = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200µA (e.g. L6385 and L6386 (L6384 → 100µA)), so if HVG T_{ON} is 5ms,C_{BOOT} has to supply 1µC to C_{EXT}. This charge on a 1µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current). This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical L6384, L6385 and L6386 value: 125 Ohm). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} \cdot R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 6µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \approx 0.8V$$

V_{drop} has to be considered when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time (e.g. Fig. 13,14,15), an external diode can be used, and this is the reason for which the external diode D1 is dotted in fig 2,4 and 6.

Working at very low frequencies the high side driver is very long. So C_{BOOT} voltage can drop because of of HVG steady state consumption. To avoid extremely large capacitor (> 1-2µF) an external charge pump can be added (see fig 9 as example).The diodes used are bot high voltage ones: they are signal diodes because the high voltage drops on C1 and C2. It is mandatory the diodes to have a low parasitic capacitance, because C1 and C2 have to be greater than diodes capacitance. The oscillator has to work in order to balance the high voltage side consumption, and the minimum frequency is fixed by C1

and C2 values (with C1,2 33pF f>250-300KHz). Moreover the oscillator has to be able to sustain the dV/dt of the OUT pin.

Figure 8. Bootstrap Driver

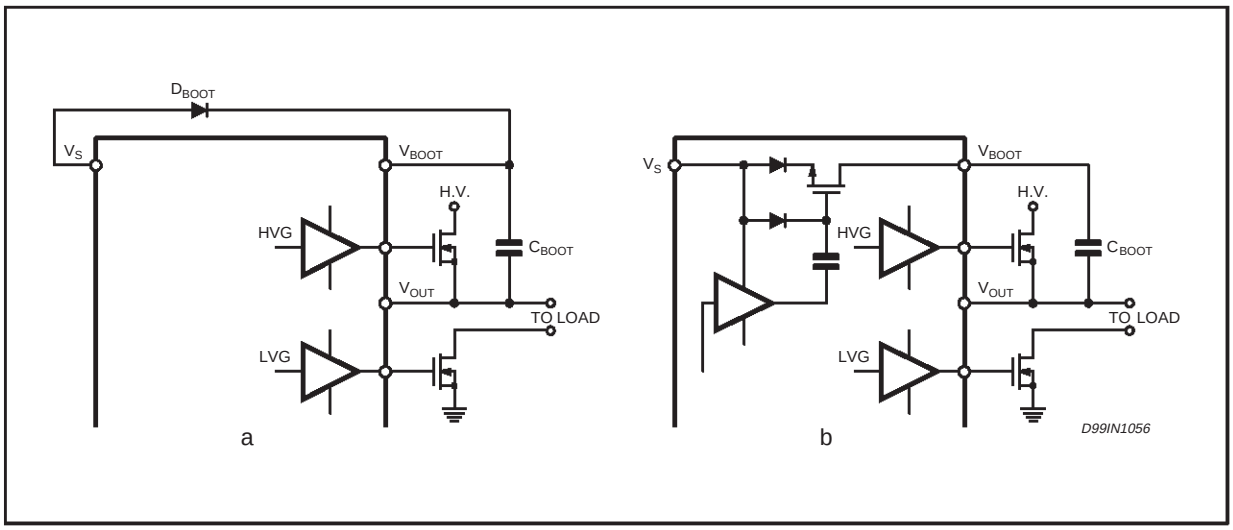
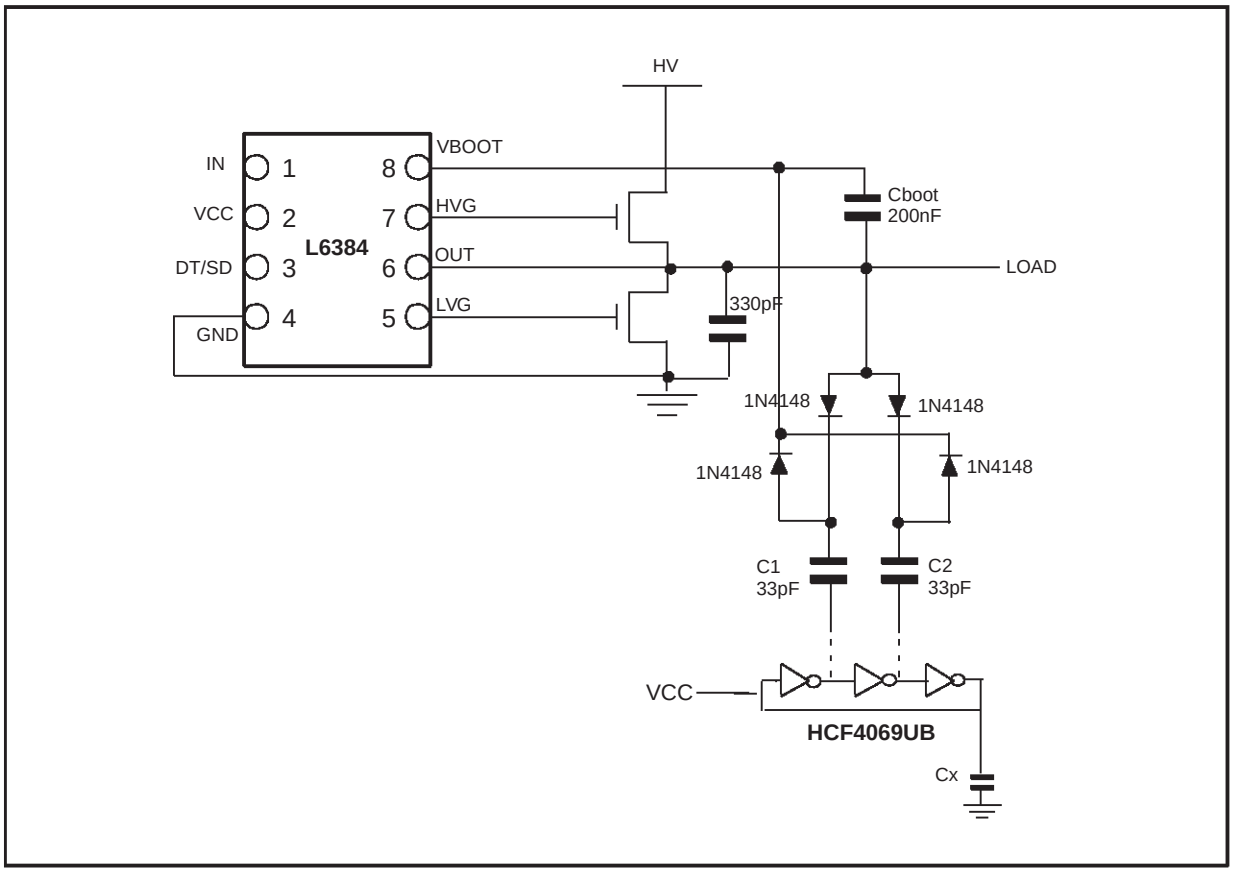


Figure 9. External Charge Pump



APPLICATION IDEAS

Here below, follows a collection of application hints that highlight the versatility and flexibility of this family of High and Low side drivers. Moreover their simplicity and compactness make these devices a cost effective solution.

For further information on these ICs, please refer to:

AN1263: "Using the internal bootstrap current capability of the L6384, L6385 & L6386 in driving a six transistor inverter bridge" by D. Nolan.

AN1299: "L6384, L6385, L6386 & L6387 tricks and tips" by P. Meloncelli.

Figure 10. L6384 µC three-phase motor control.

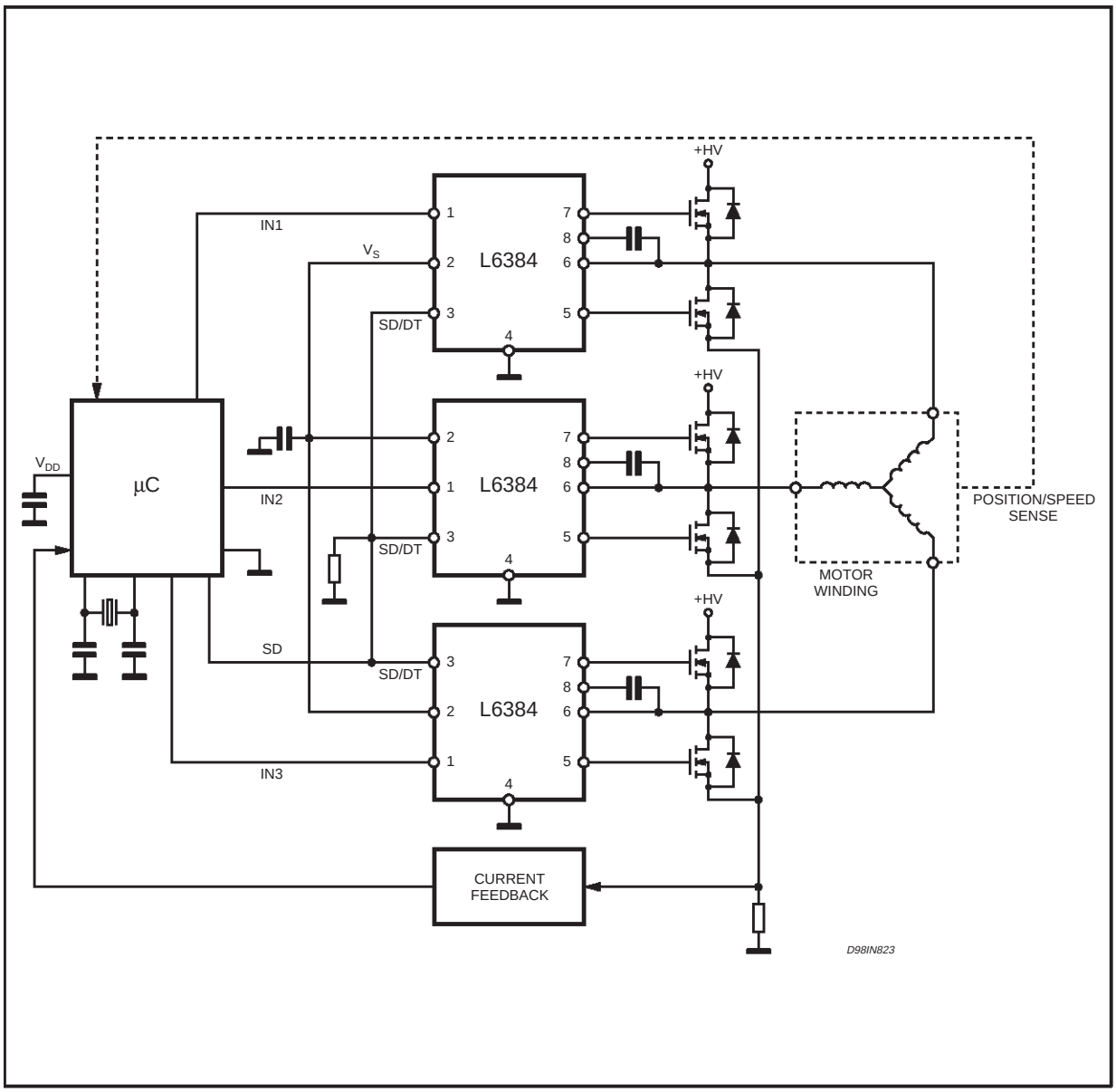


Figure 11. L6384 Dimmable lamp ballast.

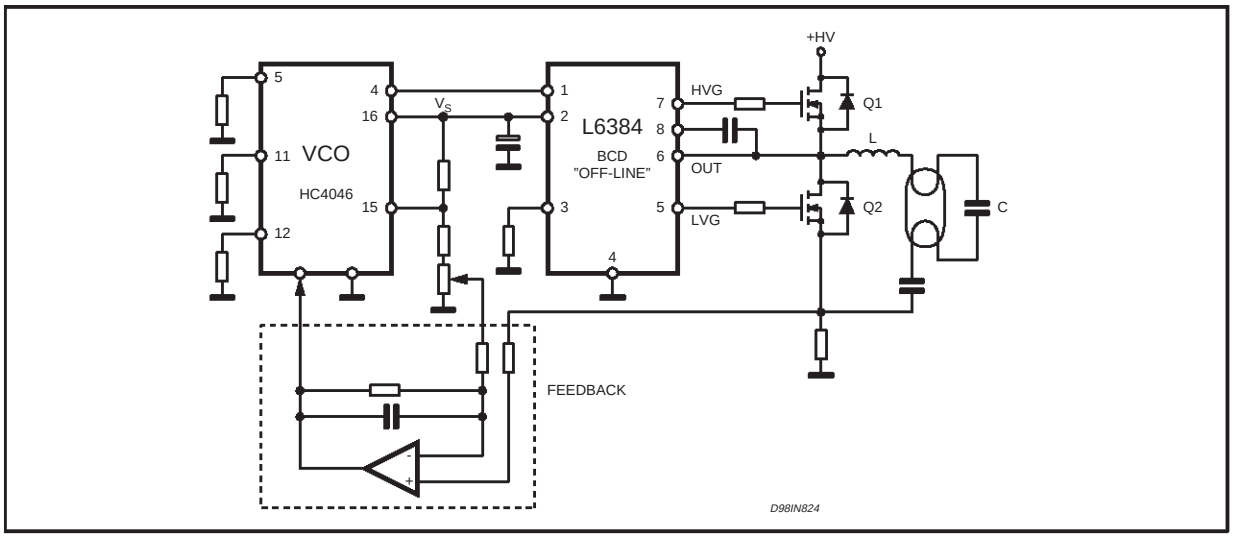


Figure 12. L6384 Half Bridge Converter

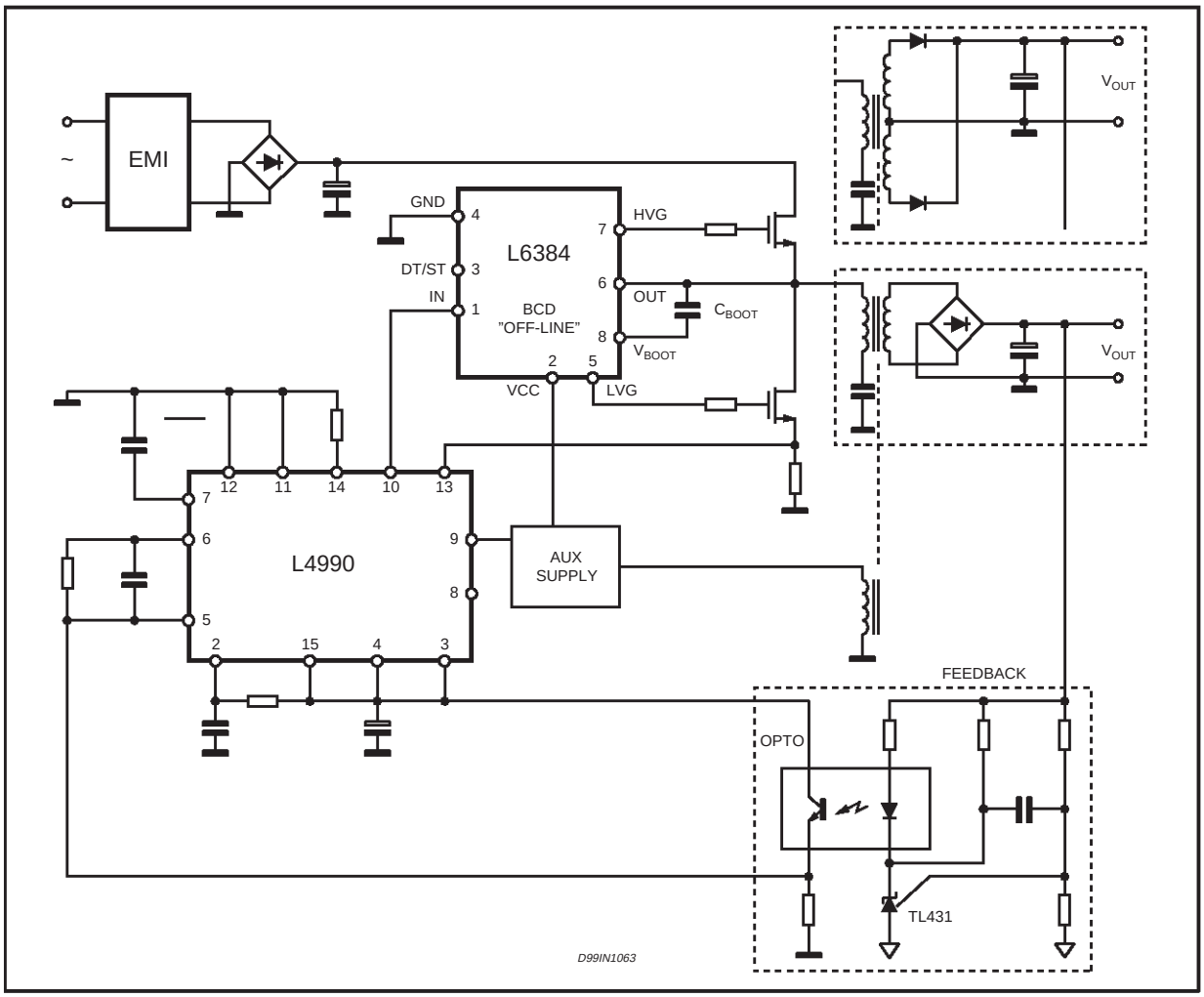


Figure 13. L6385 Horizontal deflection stage.

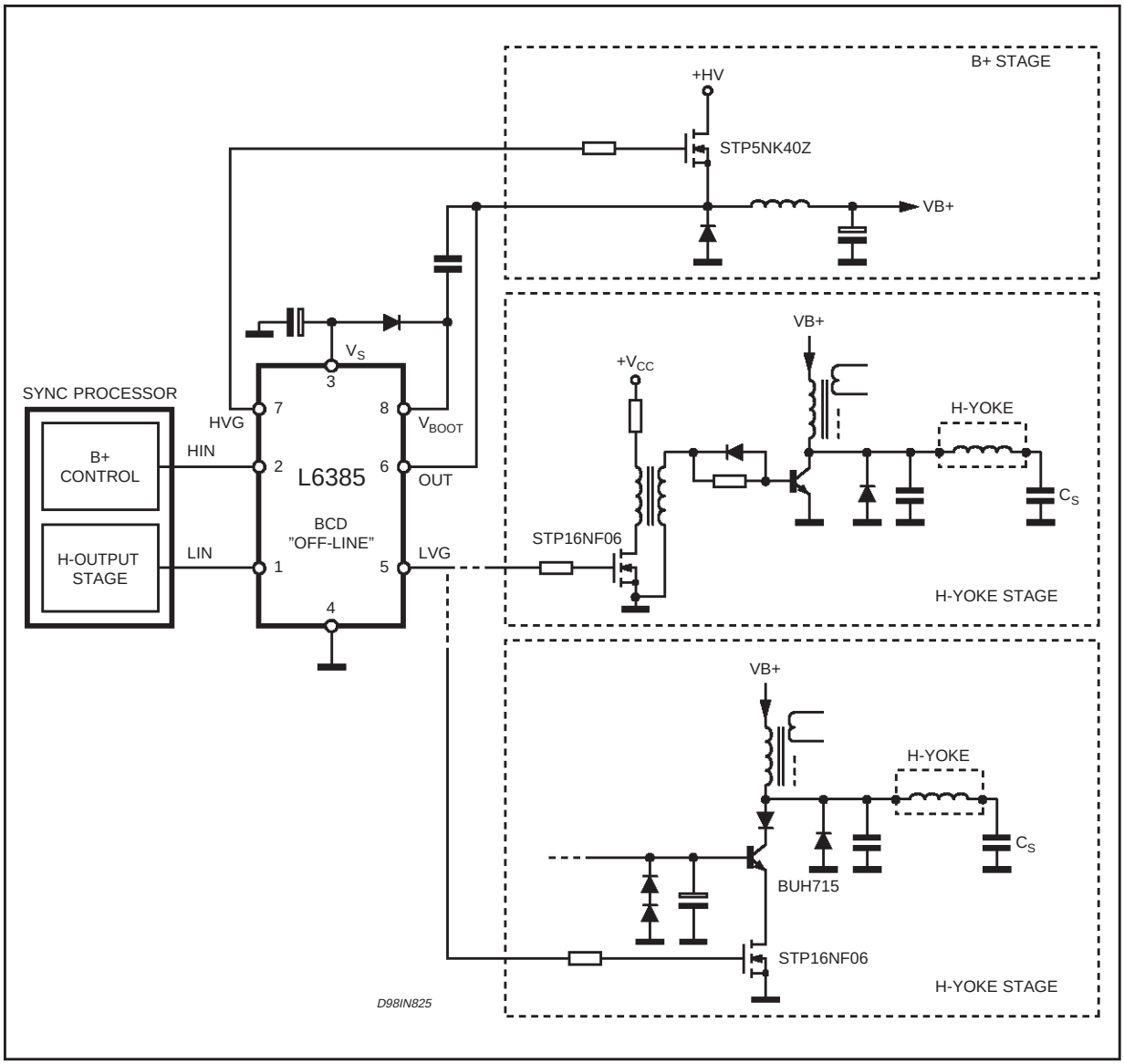


Figure 14. L6385 Two switch forward converter.

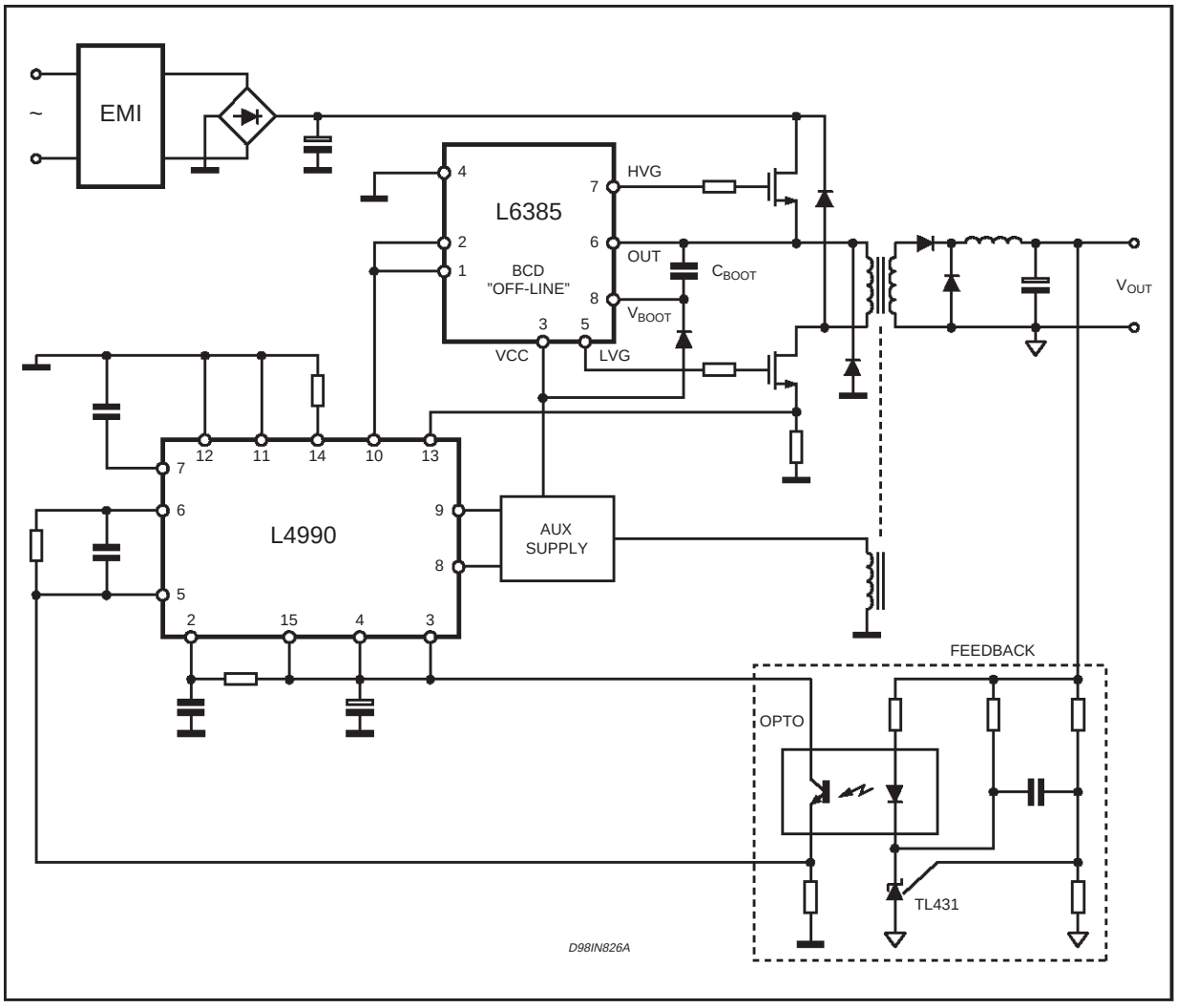


Figure 15. L6385 Asymmetrical half bridge.

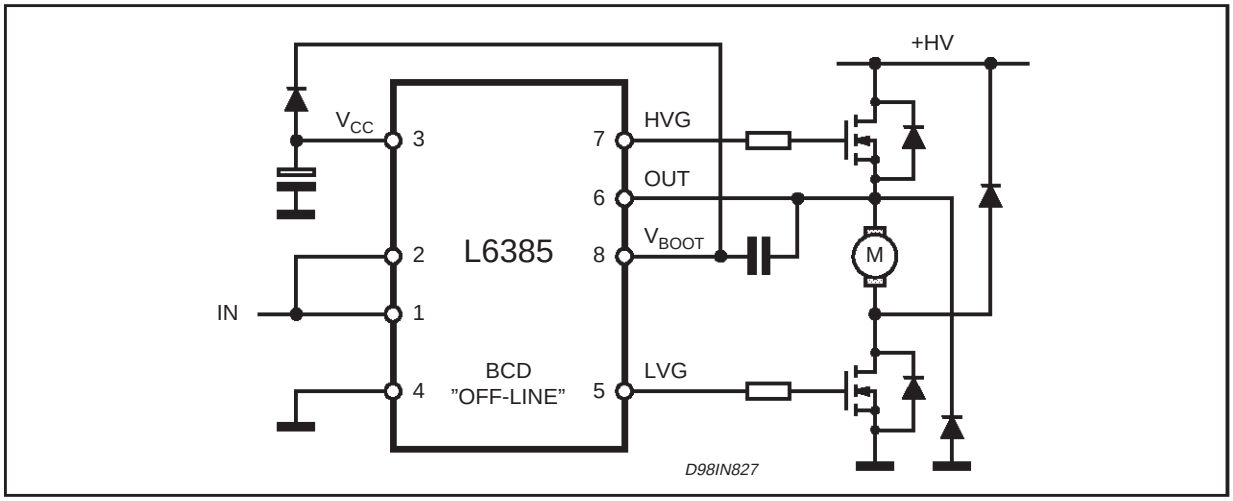
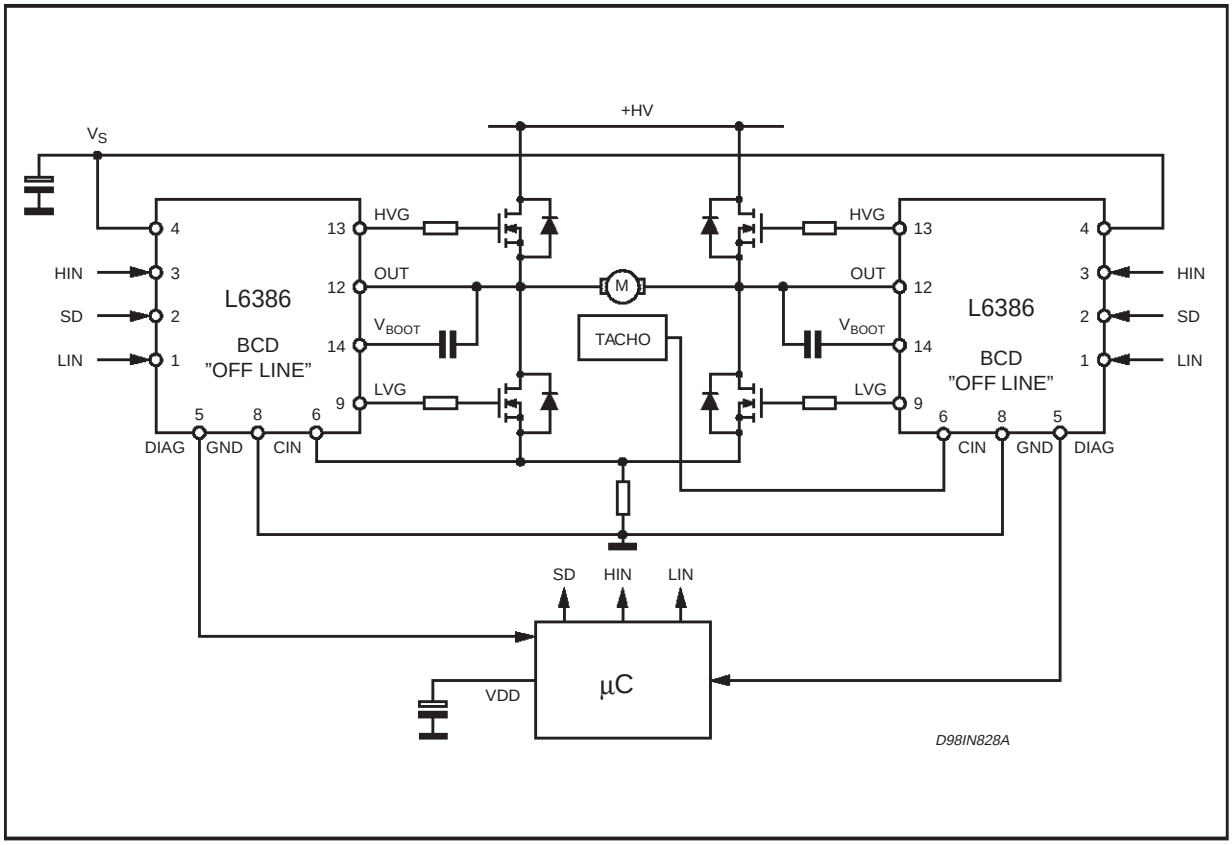


Figure 16. L6386 H-bridge with cycle by cycle control.



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