

LME49860 44V Dual High Performance, High Fidelity Audio Operational Amplifier

Check for Samples: [LME49860](#), [LME49860MABD](#), [LME49860NABD](#)

FEATURES

- Easily Drives 600Ω Loads
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection
- PSRR and CMRR Exceed 120dB (Typ)
- SOIC or PDIP Packages

APPLICATIONS

- Ultra High Quality Audio Amplification
- High Fidelity Preamplifiers
- High Fidelity Multimedia
- State of the Art Phono Pre Amps
- High Performance Professional Audio
- High Fidelity Equalization and Crossover Networks
- High Performance Line Drivers
- High Performance Line Receivers
- High Fidelity Active Filters

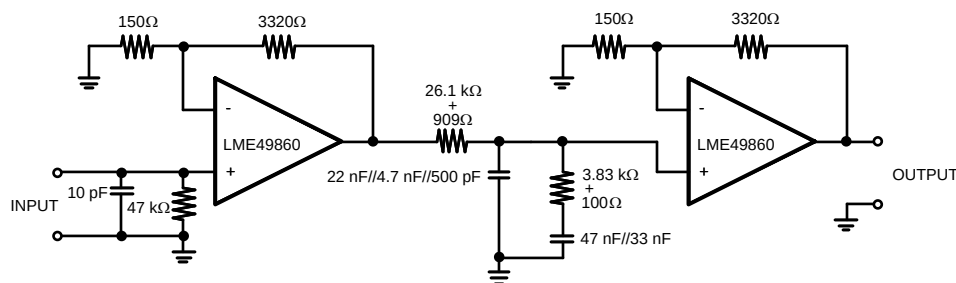
KEY SPECIFICATIONS

- Power Supply Voltage Range: ± 2.5 to $\pm 22V$
- THD+N ($A_V = 1$, $V_{OUT} = 3V_{RMS}$, $f_{IN} = 1kHz$)
 - $R_L = 2k\Omega$: 0.00003% (Typ)
 - $R_L = 600\Omega$: 0.00003% (Typ)
- Input Noise Density: 2.7 nV/ $\sqrt{Hz}$ (Typ)
- Slew Rate: $\pm 20V/\mu s$ (Typ)
- Gain Bandwidth Product: 55MHz (Typ)
- Open Loop Gain ($R_L = 600\Omega$): 140dB (Typ)
- Input Bias Current: 10nA (Typ)
- Input Offset Voltage: 0.1mV (Typ)
- DC Gain Linearity Error: 0.000009%

DESCRIPTION

The LME49860 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49860 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49860 combines extremely low voltage noise density (2.7nV/ $\sqrt{Hz}$) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications.

TYPICAL APPLICATION



Note: 1% metal film resistors, 5% polypropylene capacitors

Figure 1. Passively Equalized RIAA Phono Preamplifier



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DESCRIPTION (CONTINUED)

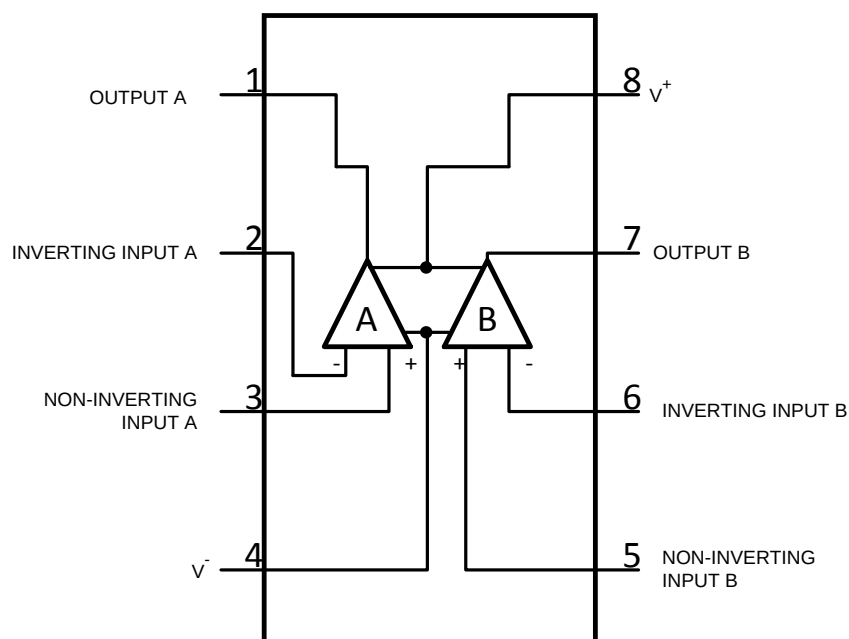
To ensure that the most challenging loads are driven without compromise, the LME49860 has a high slew rate of $\pm 20\text{V}/\mu\text{s}$ and an output current capability of $\pm 26\text{mA}$. Further, dynamic range is maximized by an output stage that drives $2\text{k}\Omega$ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

The LME49860's outstanding CMRR (120dB), PSRR (120dB), and V_{OS} (0.1mV) give the amplifier excellent operational amplifier DC performance.

The LME49860 has a wide supply range of $\pm 2.5\text{V}$ to $\pm 22\text{V}$. Over this supply range the LME49860 maintains excellent common-mode rejection, power supply rejection, and low input bias current. The LME49860 is unity gain stable. This Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with values as high as 100pF .

The LME49860 is available in 8-lead narrow body SOIC and 8-lead PDIP packages. Demonstration boards are available for each package.

Connection Diagrams



**Figure 2. 8-Pin SOIC or PDIP
See D or P Package**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

Power Supply Voltage ($V_S = V^+ - V^-$)		46V
Storage Temperature		-65°C to 150°C
Input Voltage		(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit ⁽⁴⁾		Continuous
ESD Susceptibility ⁽⁵⁾		2000V
ESD Susceptibility ⁽⁶⁾	Pins 1, 4, 7 and 8	200V
	Pins 2, 3, 5 and 6	100V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (SOIC)	145°C/W
	θ_{JA} (PDIP)	102°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
- (2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instrument Sales Office/ Distributors for availability and specifications.
- (4) Amplifier output connected to GND, any number of amplifiers within a package.
- (5) Human body model, 100pF discharged through a 1.5kΩ resistor.
- (6) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

OPERATING RATINGS

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C ≤ T_A ≤ 85°C
Supply Voltage Range		±2.5V ≤ V_S ≤ ±22V

ELECTRICAL CHARACTERISTICS FOR THE LME49860⁽¹⁾

The following specifications apply for $V_S = \pm 18V$ and $\pm 22V$, $R_L = 2k\Omega$, $R_{SOURCE} = 10\Omega$, $f_{IN} = 1kHz$, $T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	LME49860		Units (Limits)
			Typical ⁽²⁾	Limit ⁽³⁾	
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$, $V_{OUT} = 3V_{rms}$ $R_L = 2k\Omega$ $R_L = 600\Omega$	0.00003 0.00003	0.00009	% (max)
IMD	Intermodulation Distortion	$A_V = 1$, $V_{OUT} = 3V_{RMS}$, Two-tone, 60Hz & 7kHz 4:1	0.00005		%
GBWP	Gain Bandwidth Product		55	45	MHz (min)
SR	Slew Rate		±20	±15	V/μs (min)
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}$, -3dB referenced to output magnitude at $f = 1kHz$	10		MHz
t_s	Settling time	$A_V = -1$, 10V step, $C_L = 100pF$, 0.1% error range	1.2		μs
e_n	Equivalent Input Noise Voltage	$f_{BW} = 20Hz$ to 20kHz	0.34	0.65	μV _{RMS} (max)
	Equivalent Input Noise Density	$f = 1kHz$ $f = 10Hz$	2.7 6.4	4.7	nV/√Hz (max)
i_n	Current Noise Density	$f = 1kHz$ $f = 10Hz$	1.6 3.1		pA/√Hz (max)
V_{OS}	Offset Voltage	$V_S = \pm 18V$	±0.12	±0.7	mV (max)
		$V_S = \pm 22V$	±0.14	±0.7	mV (max)
$\Delta V_{OS}/\Delta T_{mp}$	Average Input Offset Voltage Drift vs Temperature	-40°C ≤ T_A ≤ 85°C	0.2		μV/°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
- (2) Typical specifications are specified at +25°C and represent the most likely parametric norm.
- (3) Tested limits are ensured to AOQL (Average Outgoing Quality Level).

ELECTRICAL CHARACTERISTICS FOR THE LME49860⁽¹⁾ (continued)

The following specifications apply for $V_S = \pm 18V$ and $\pm 22V$, $R_L = 2k\Omega$, $R_{SOURCE} = 10\Omega$, $f_{IN} = 1kHz$, $T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	LME49860		Units (Limits)
			Typical ⁽²⁾	Limit ⁽³⁾	
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	See ⁽⁴⁾ $V_S = \pm 18V$, $\Delta V_S = 24V$ $V_S = \pm 22V$, $\Delta V_S = 30V$	120 120	110	dB dB (min)
ISO _{CH-CH}	Channel-to-Channel Isolation	$f_{IN} = 1kHz$ $f_{IN} = 20kHz$	118 112		dB
I _B	Input Bias Current	$V_{CM} = 0V$	10	72	nA (max)
$\Delta I_{OS}/\Delta T_{emp}$	Input Bias Current Drift vs Temperature	$-40^\circ C \leq T_A \leq 85^\circ C$	0.1		nA/ $^\circ C$
I _{OS}	Input Offset Current	$V_{CM} = 0V$	11	65	nA (max)
V _{IN-CM}	Common-Mode Input Voltage Range	$V_S = \pm 18V$	+17.1 -16.9	(V+) – 2.0 (V-) + 2.0	V (min) V (min)
		$V_S = \pm 22V$	+21.0 -20.8	(V+) – 2.0 (V-) + 2.0	V (min) V (min)
CMRR	Common-Mode Rejection	$V_S = \pm 18V$ $-12V \leq V_{CM} \leq 12V$	120		dB
		$V_S = \pm 22V$ $-15V \leq V_{CM} \leq 15V$	120	110	dB (min)
Z _{IN}	Differential Input Impedance		30		k Ω
	Common Mode Input Impedance	$-10V < V_{CM} < 10V$	1000		M Ω
A _{VOL}	Open Loop Voltage Gain	$V_S = \pm 18V$ $-12V \leq V_{out} \leq 12V$ $R_L = 600\Omega$ $R_L = 2k\Omega$ $R_L = 10k\Omega$	140 140 140		dB dB dB
		$V_S = \pm 22V$ $-15V \leq V_{out} \leq 15V$ $R_L = 600\Omega$ $R_L = 2k\Omega$ $R_L = 10k\Omega$	140 140 140	125	dB (min) dB dB
V _{OUTMAX}	Maximum Output Voltage Swing	$R_L = 600\Omega$ $V_S = \pm 18V$ $V_S = \pm 22V$	± 16.7 ± 20.4	± 19.0	V V (min)
		$R_L = 2k\Omega$ $V_S = \pm 18V$ $V_S = \pm 22V$	± 17.0 ± 21.0		V V
		$R_L = 10k\Omega$ $V_S = \pm 18V$ $V_S = \pm 22V$	± 17.1 ± 21.2		V V
I _{OUT}	Output Current	$R_L = 600\Omega$ $V_S = \pm 20V$ $V_S = \pm 22V$	± 31 ± 37	± 30	mA mA (min)
I _{OUT-CC}	Instantaneous Short Circuit Current		+53 -42		mA
R _{OUT}	Output Impedance	$f_{IN} = 10kHz$ Closed-Loop Open-Loop	0.01 13		Ω
C _{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I _S	Total Quiescent Current	I _{OUT} = 0mA $V_S = \pm 18V$ $V_S = \pm 22V$	10.2 10.5	13	mA mA (max)

(4) PSRR is measured as follows: For $V_S = \pm 22V$, V_{OS} is measured at two supply voltages, $\pm 7V$ and $\pm 22V$. $PSRR = |20 \log(\Delta V_{OS}/\Delta V_S)|$.

TYPICAL PERFORMANCE CHARACTERISTICS

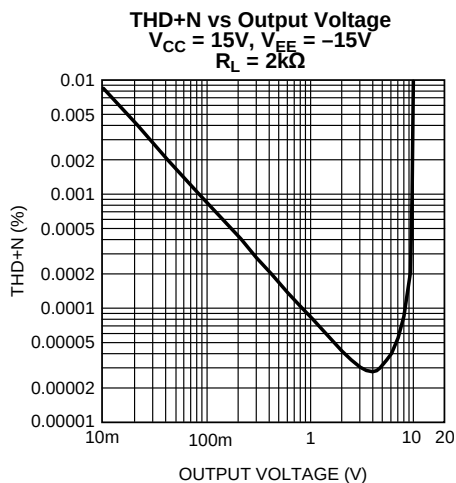


Figure 3.

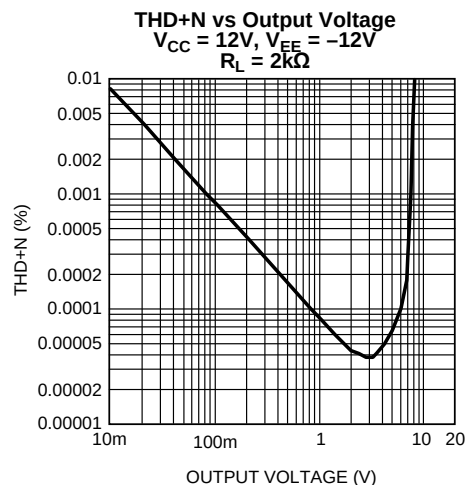


Figure 4.

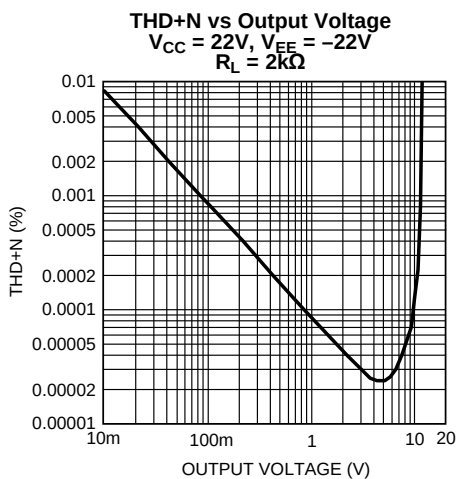


Figure 5.

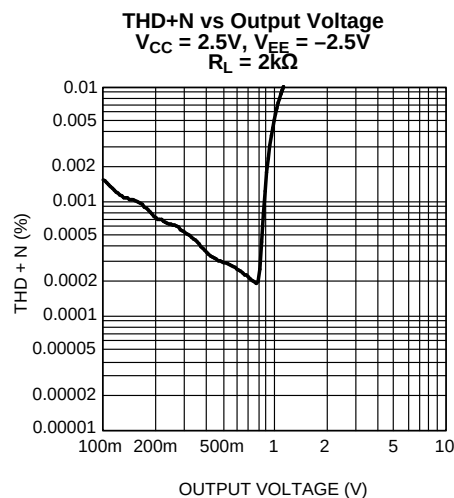


Figure 6.

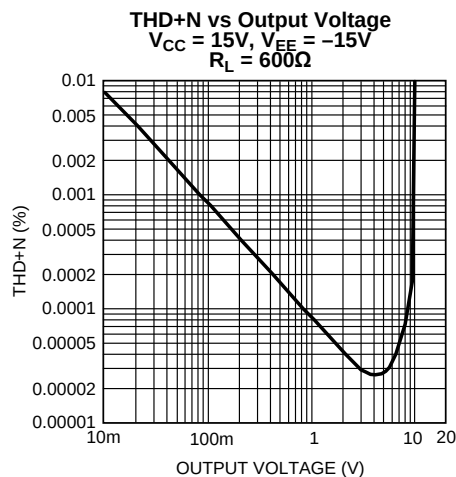


Figure 7.

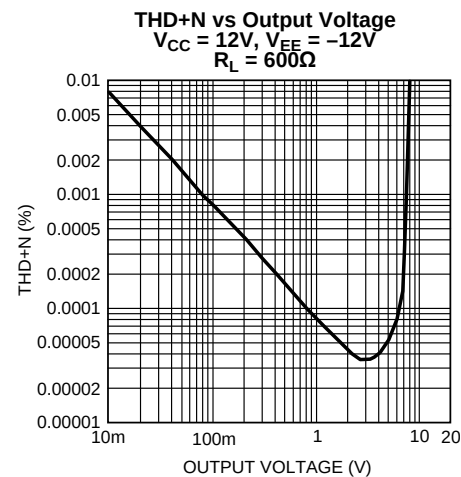
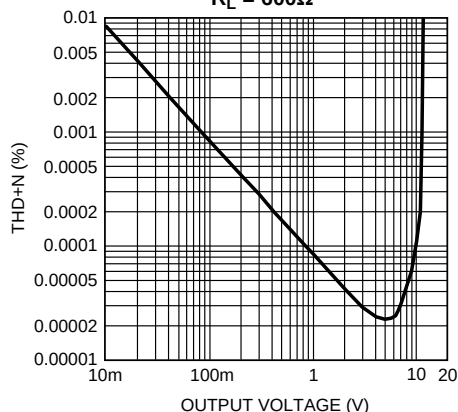


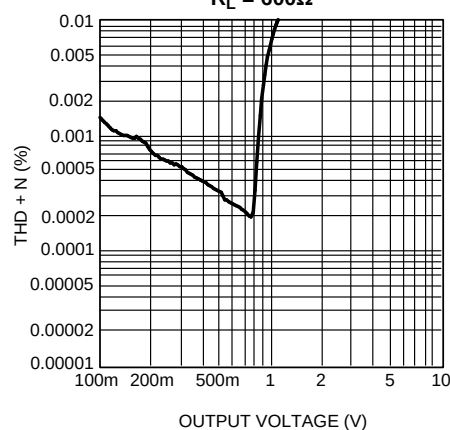
Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

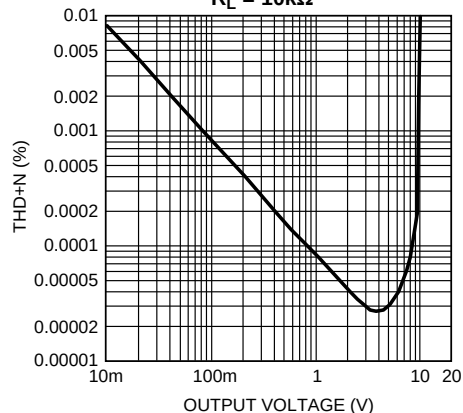
THD+N vs Output Voltage
 $V_{CC} = 22V$, $V_{EE} = -22V$
 $R_L = 600\Omega$

**Figure 9.**

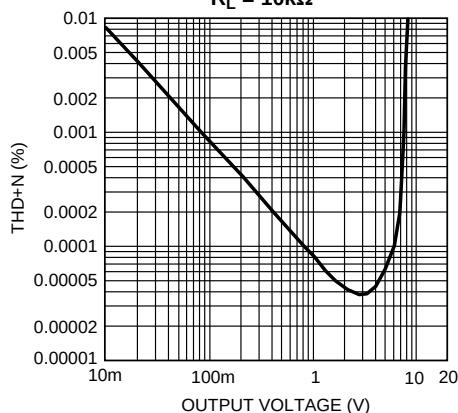
THD+N vs Output Voltage
 $V_{CC} = 2.5V$, $V_{EE} = -2.5V$
 $R_L = 600\Omega$

**Figure 10.**

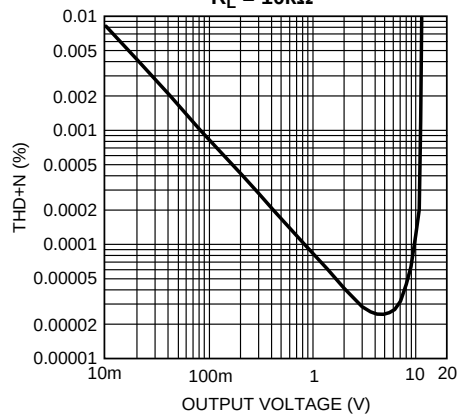
THD+N vs Output Voltage
 $V_{CC} = 15V$, $V_{EE} = -15V$
 $R_L = 10k\Omega$

**Figure 11.**

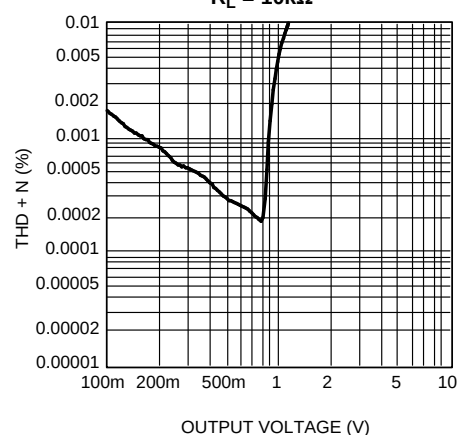
THD+N vs Output Voltage
 $V_{CC} = 12V$, $V_{EE} = -12V$
 $R_L = 10k\Omega$

**Figure 12.**

THD+N vs Output Voltage
 $V_{CC} = 22V$, $V_{EE} = -22V$
 $R_L = 10k\Omega$

**Figure 13.**

THD+N vs Output Voltage
 $V_{CC} = 2.5V$, $V_{EE} = -2.5V$
 $R_L = 10k\Omega$

**Figure 14.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

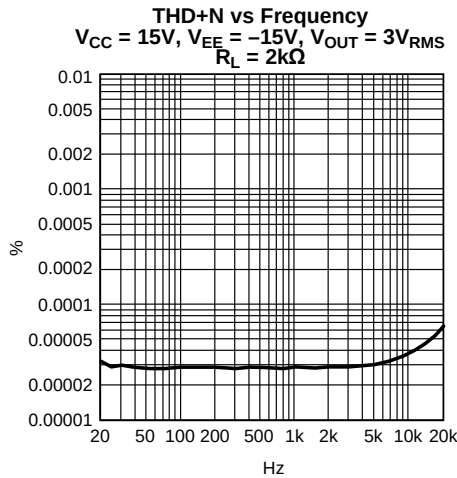


Figure 15.

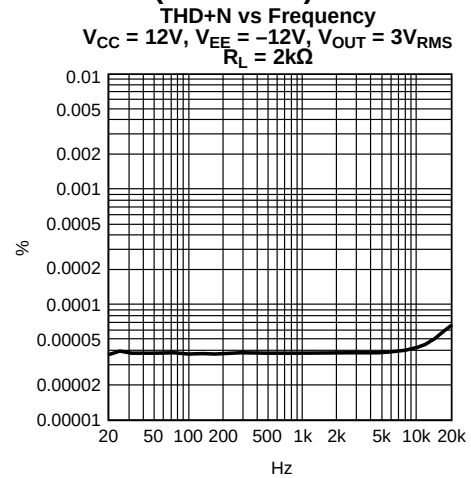


Figure 16.

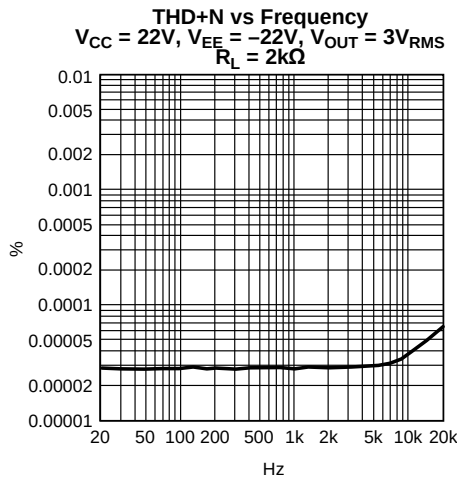


Figure 17.

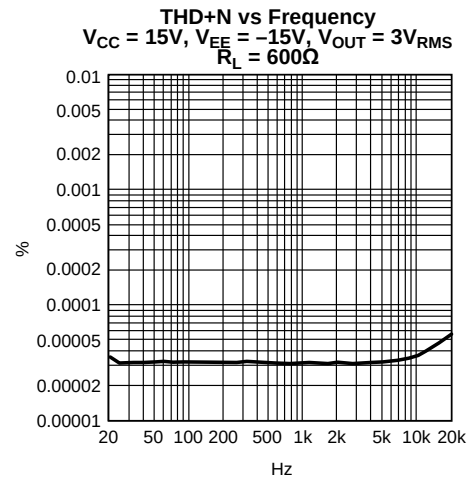


Figure 18.

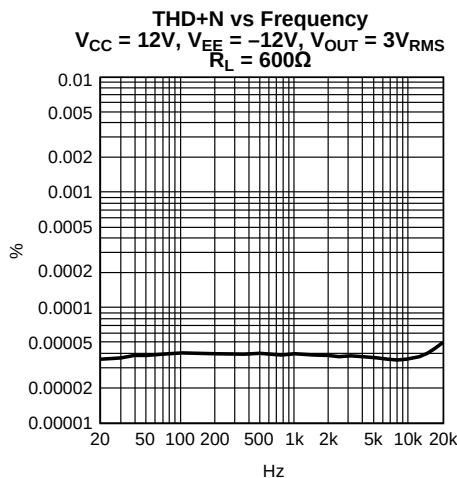


Figure 19.

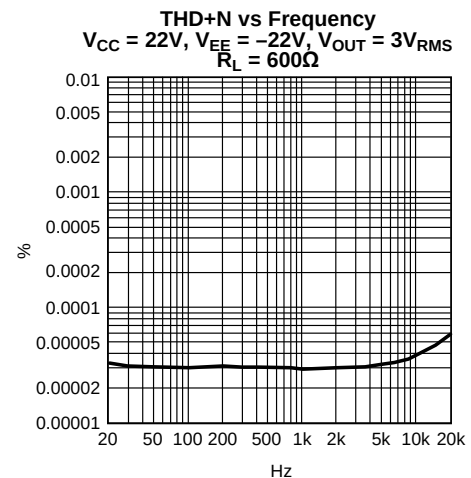
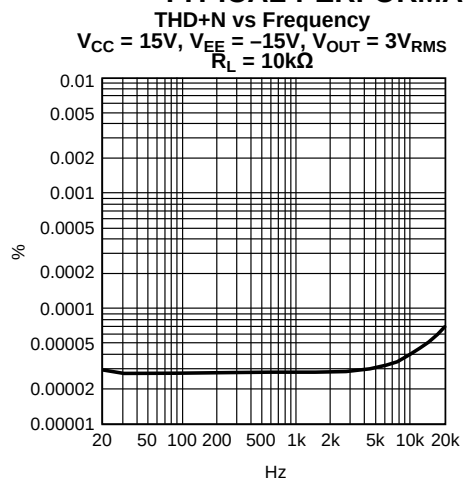
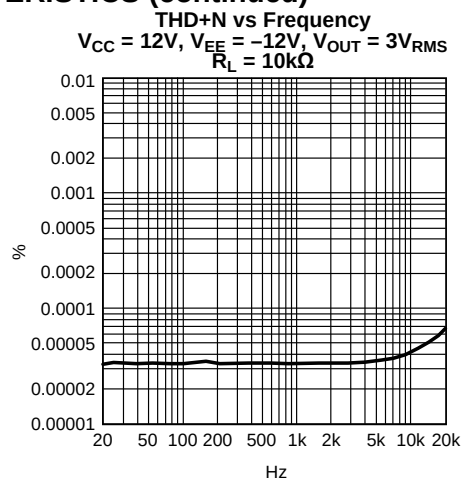
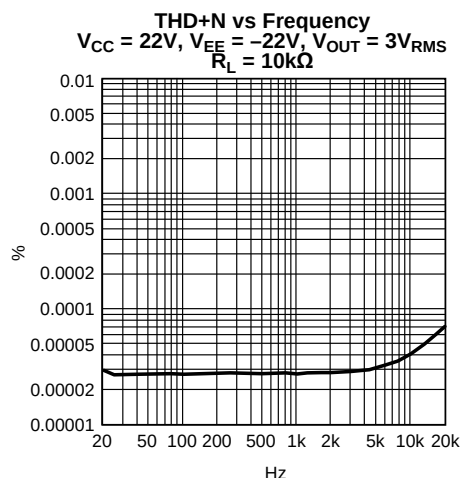
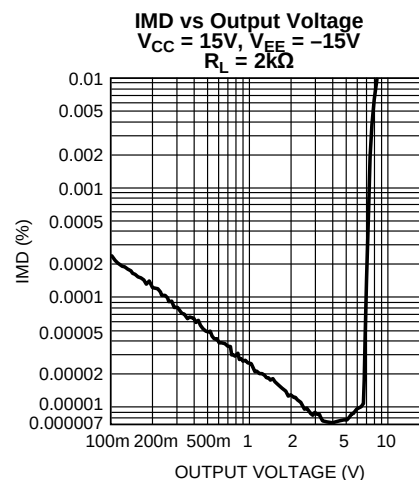
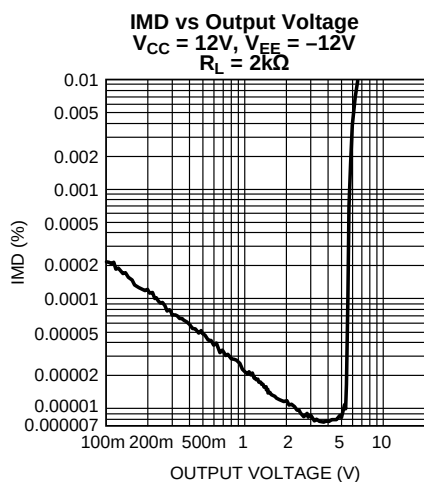
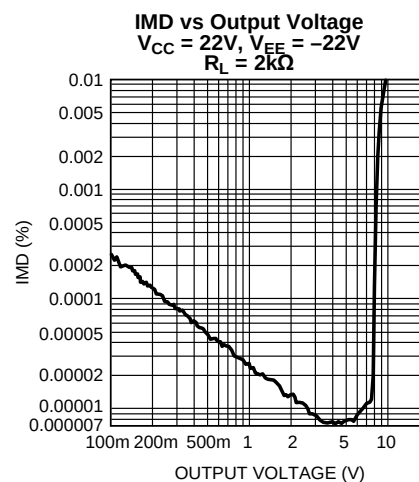


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 21.****Figure 22.****Figure 23.****Figure 24.****Figure 25.****Figure 26.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

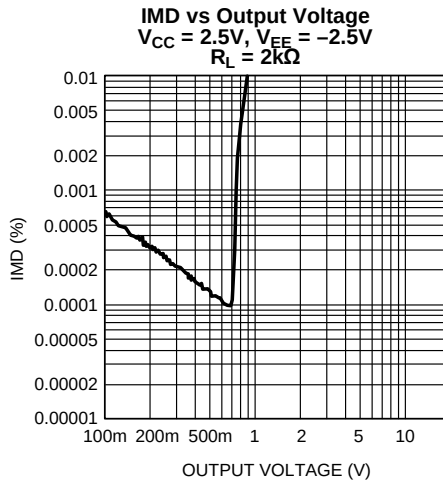


Figure 27.

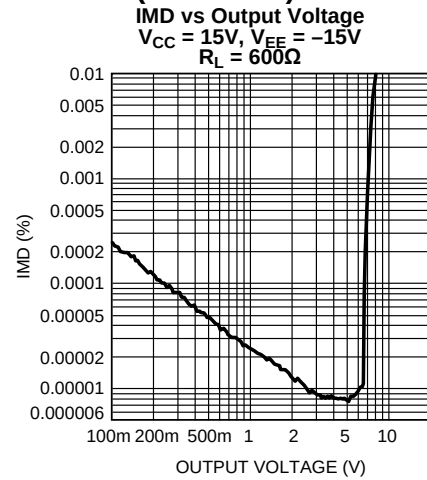


Figure 28.

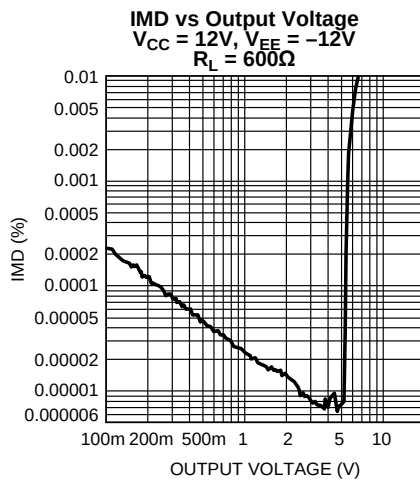


Figure 29.

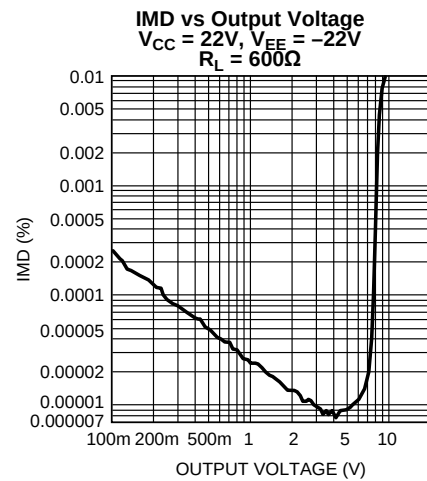


Figure 30.

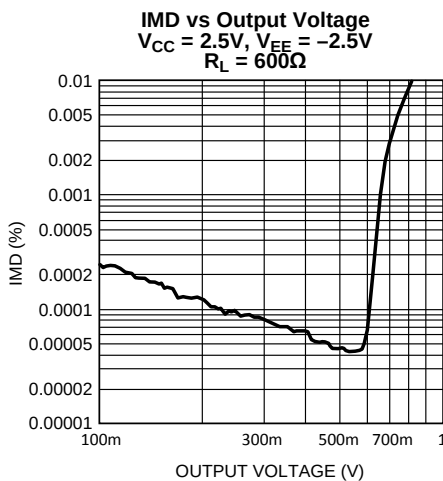


Figure 31.

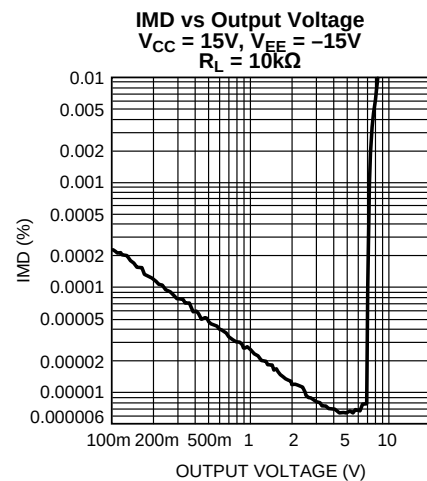
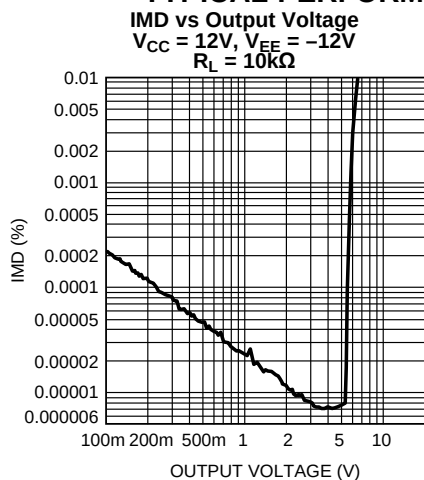
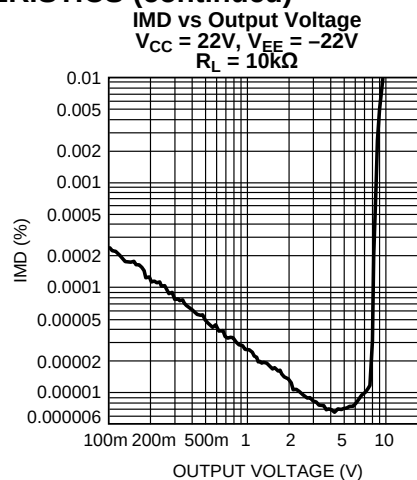
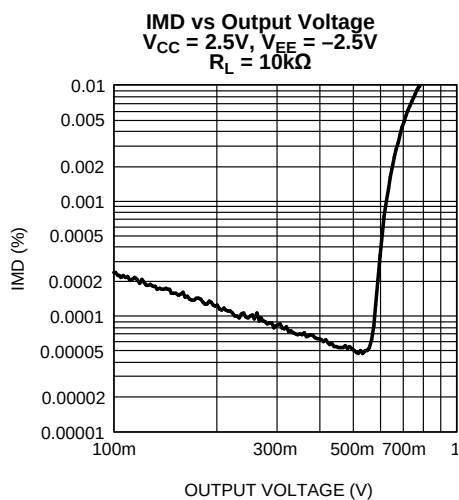
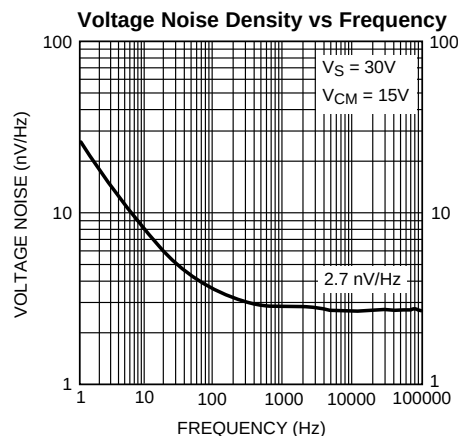
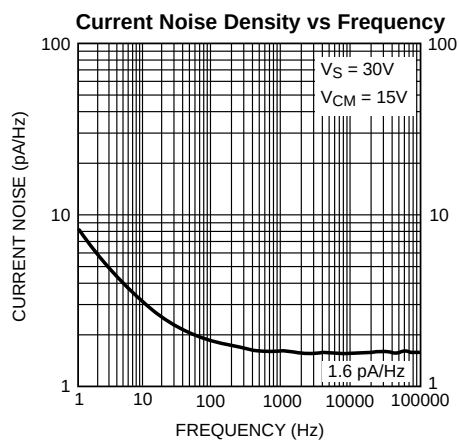
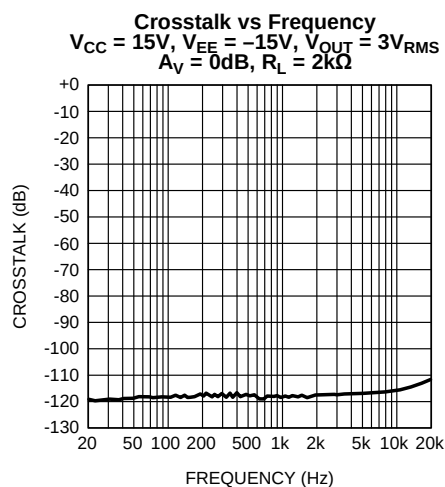


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 33.****Figure 34.****Figure 35.****Figure 36.****Figure 37.****Figure 38.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

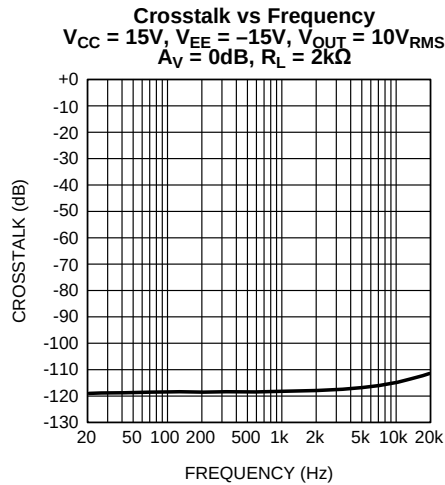


Figure 39.

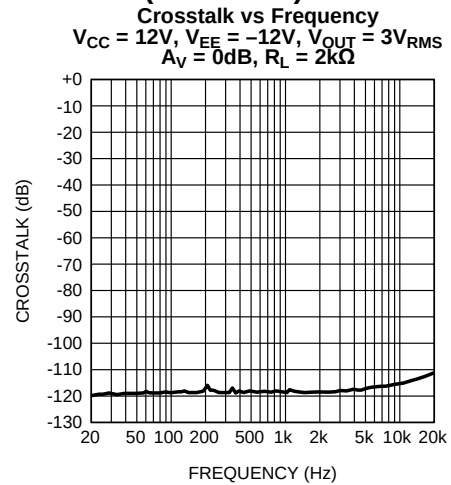


Figure 40.

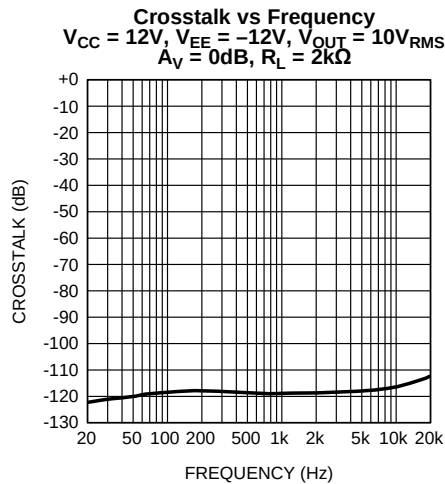


Figure 41.

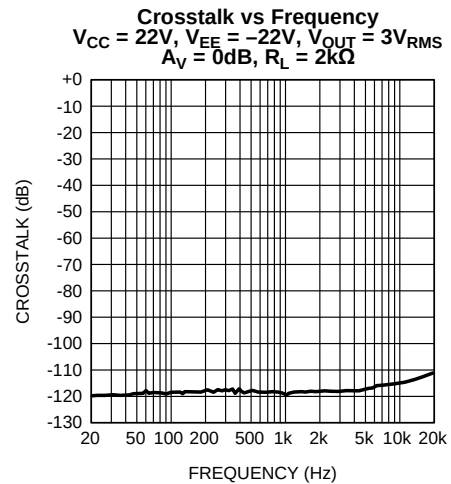


Figure 42.

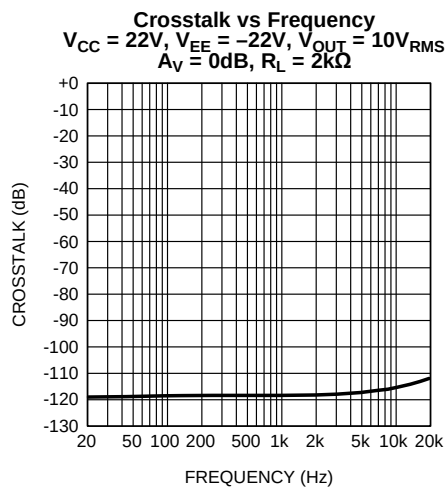


Figure 43.

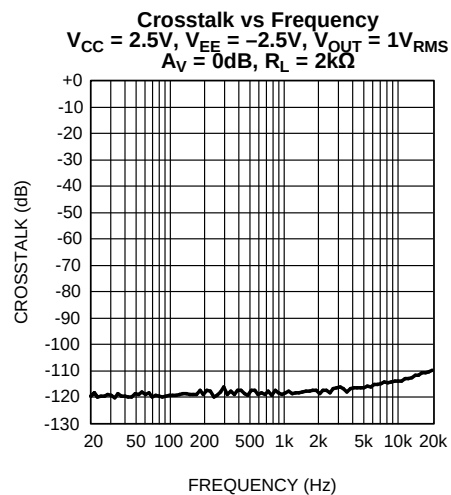
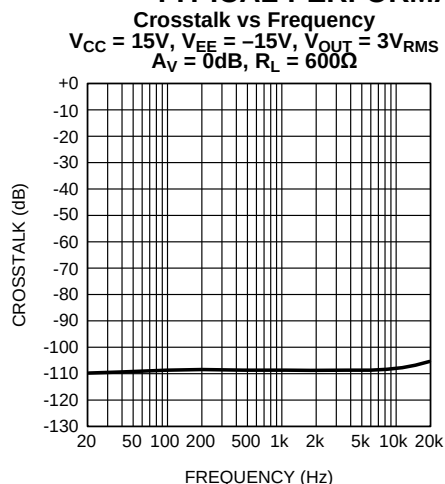
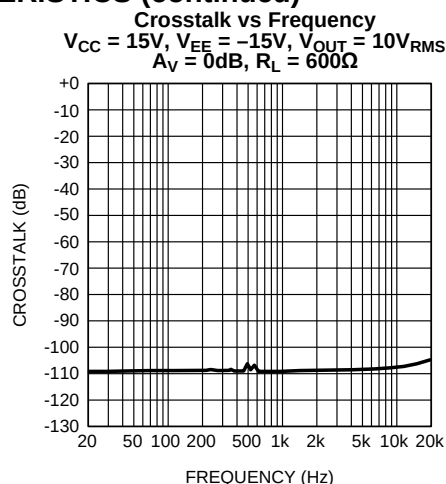
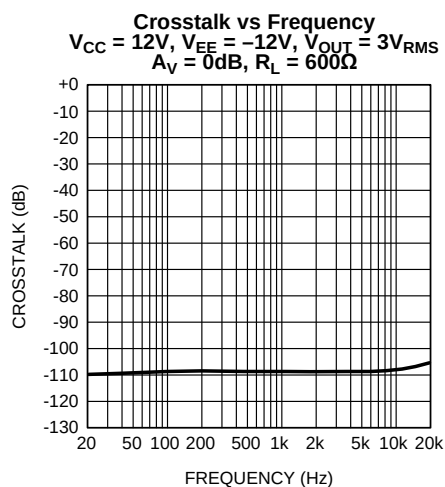
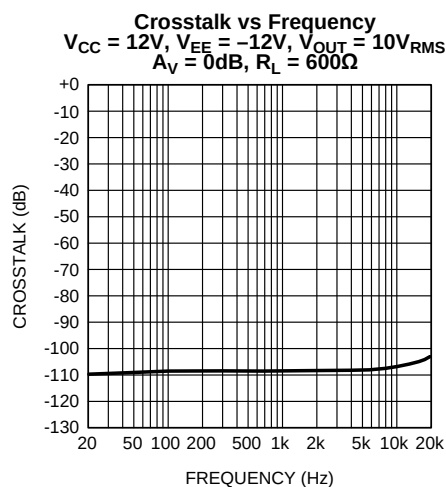
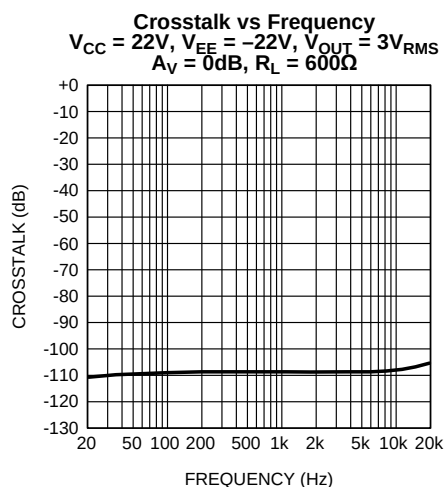
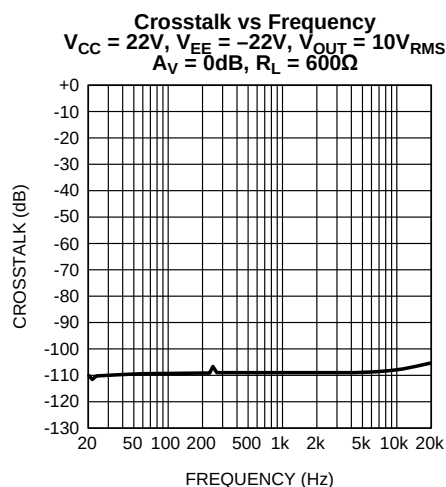


Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 45.****Figure 46.****Figure 47.****Figure 48.****Figure 49.****Figure 50.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

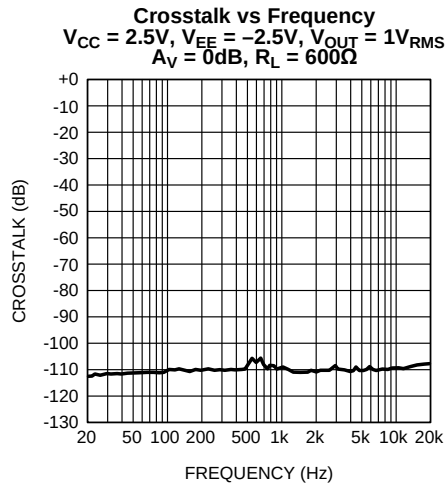


Figure 51.

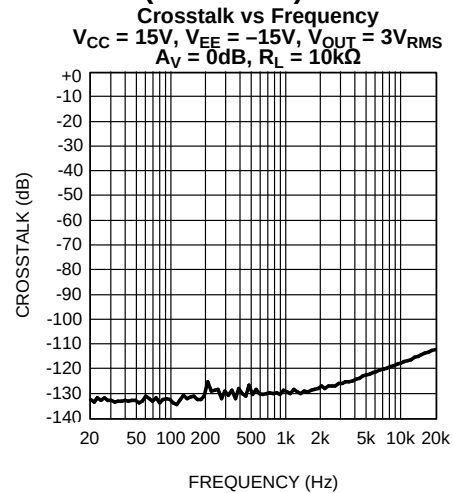


Figure 52.

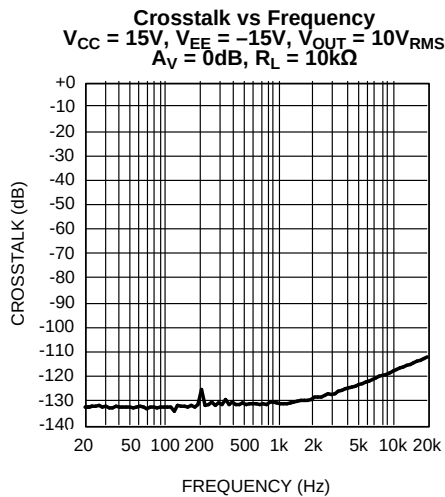


Figure 53.

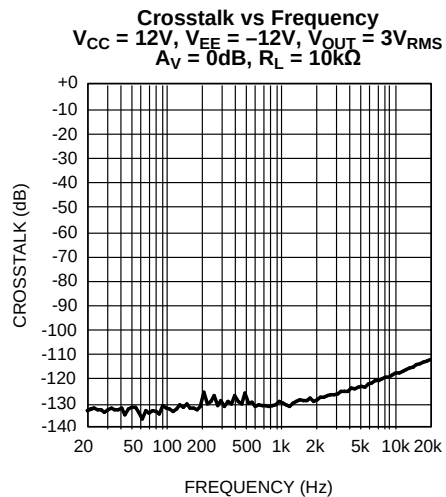


Figure 54.

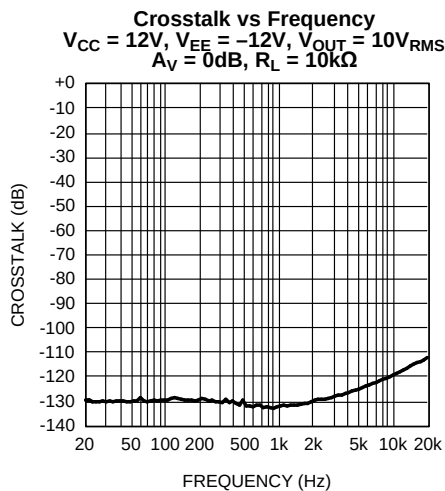


Figure 55.

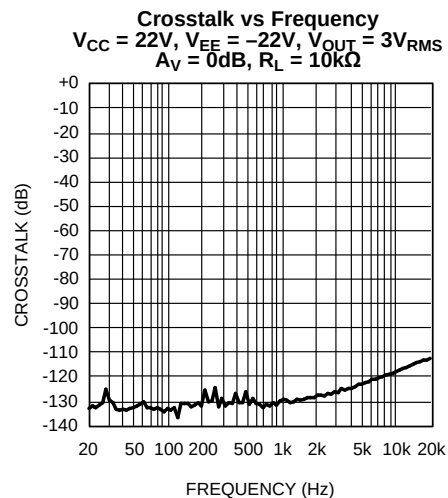
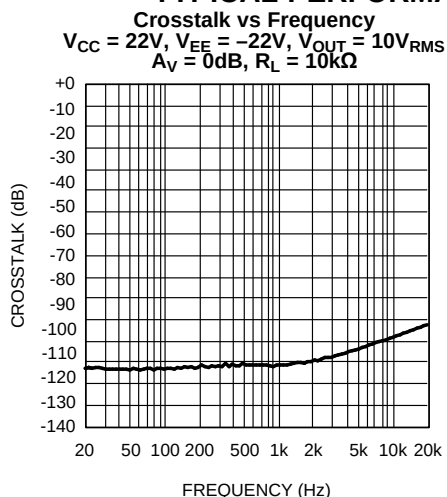
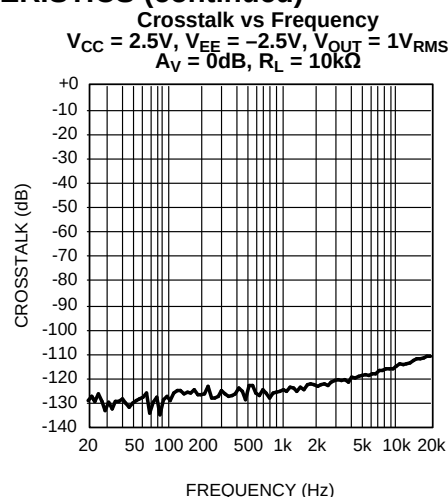
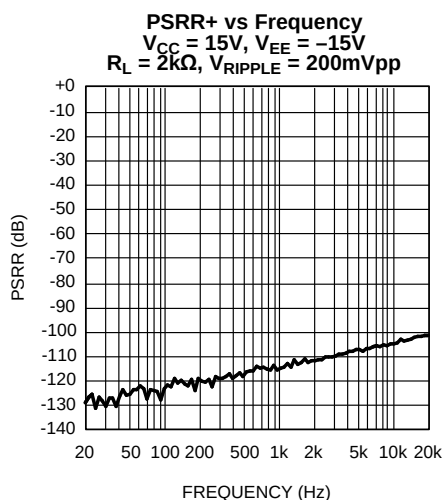
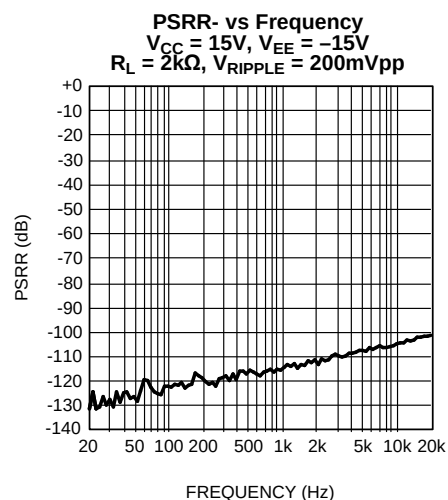
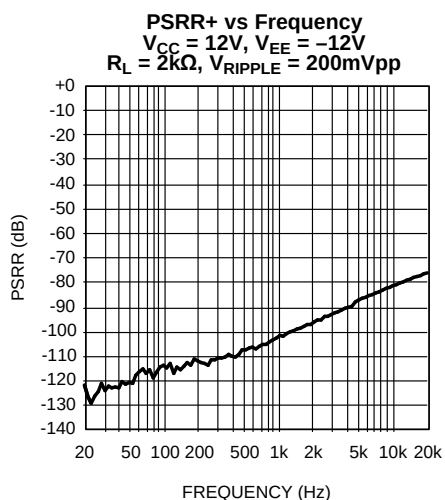
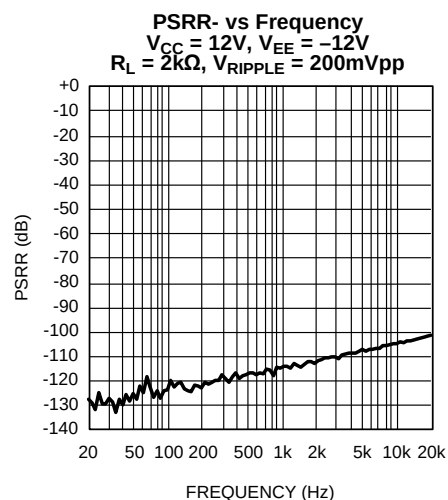


Figure 56.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 57.****Figure 58.****Figure 59.****Figure 60.****Figure 61.****Figure 62.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

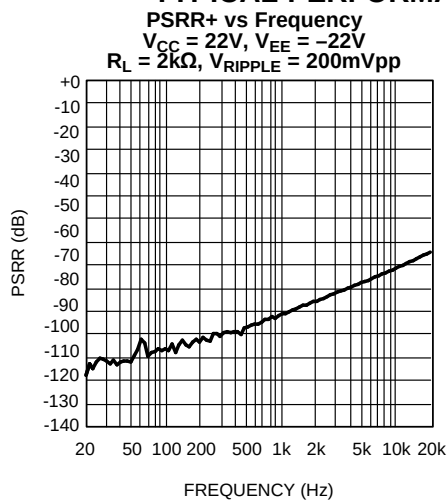


Figure 63.

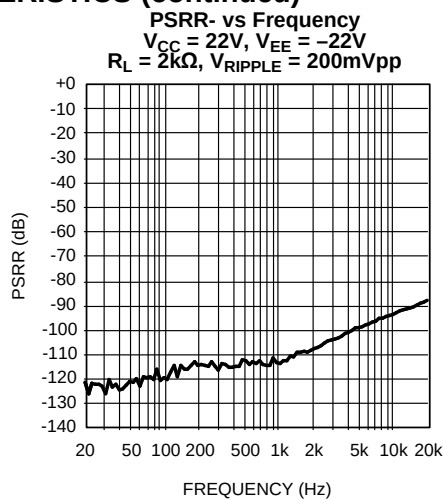


Figure 64.

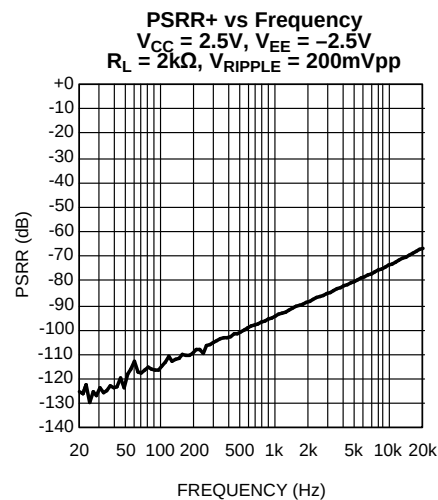


Figure 65.

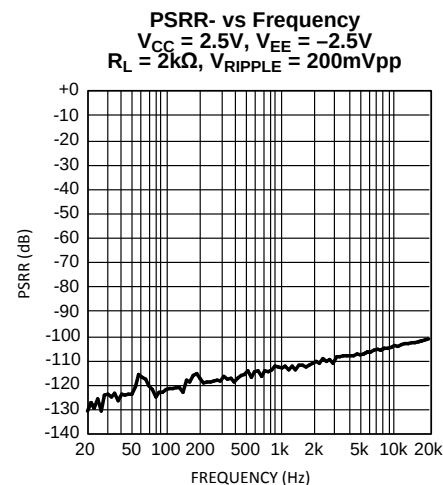


Figure 66.

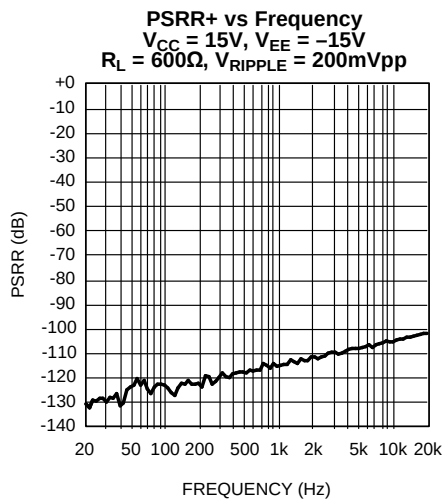


Figure 67.

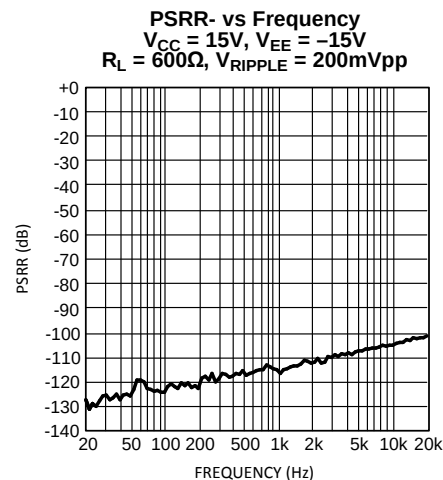
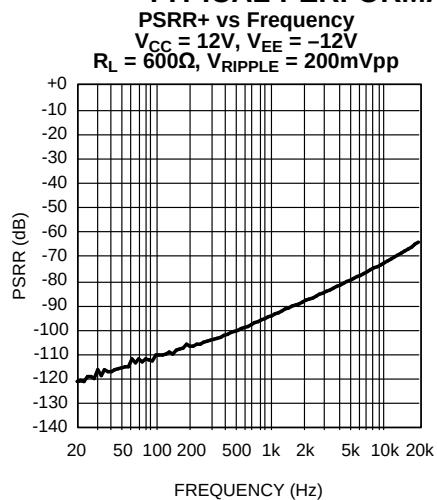
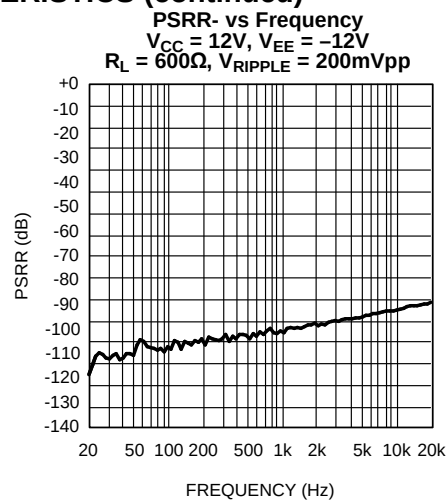
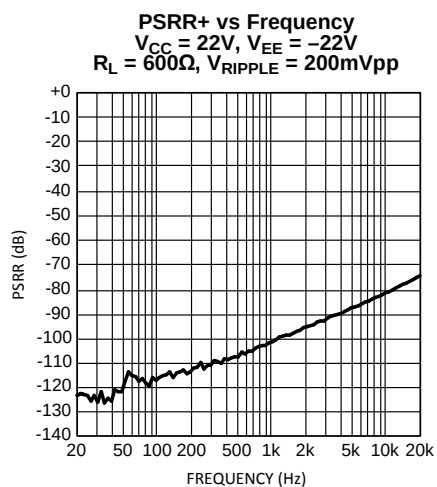
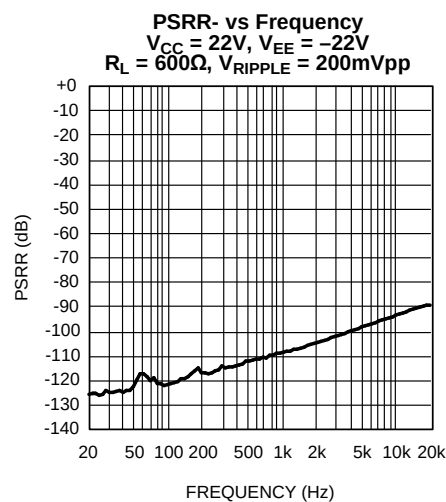
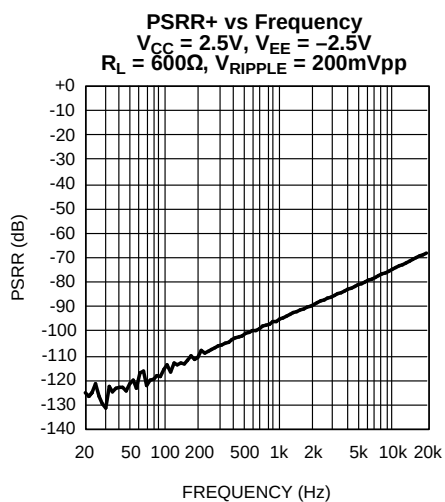
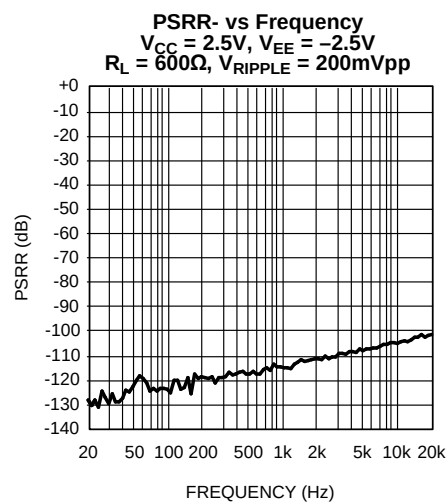


Figure 68.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 69.****Figure 70.****Figure 71.****Figure 72.****Figure 73.****Figure 74.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

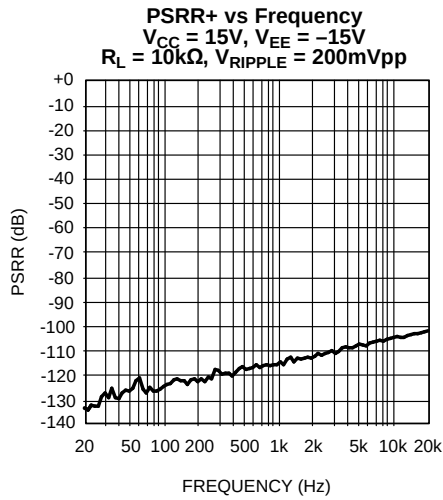


Figure 75.

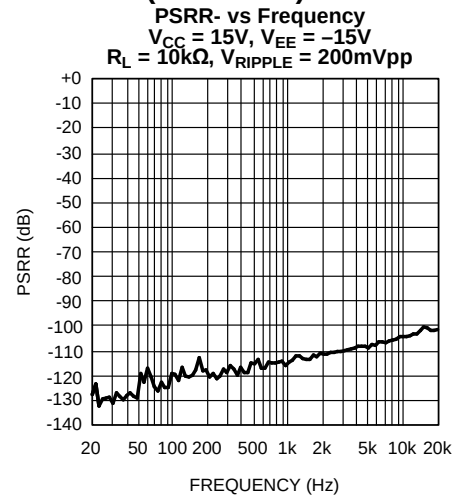


Figure 76.

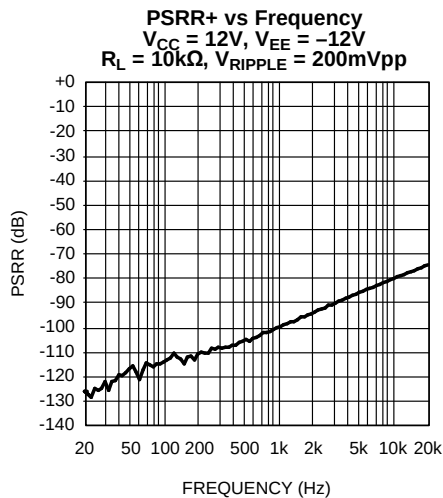


Figure 77.

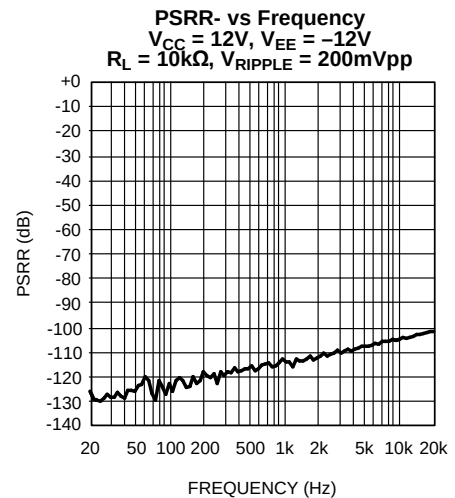


Figure 78.

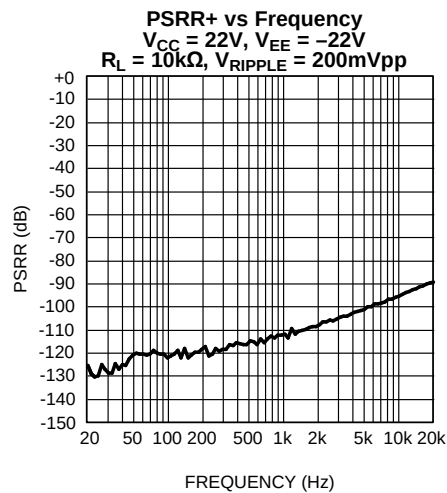


Figure 79.

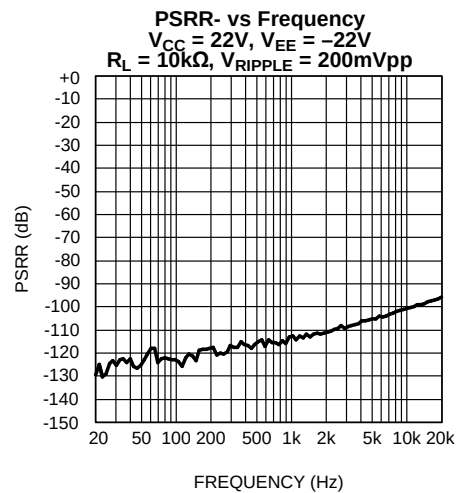
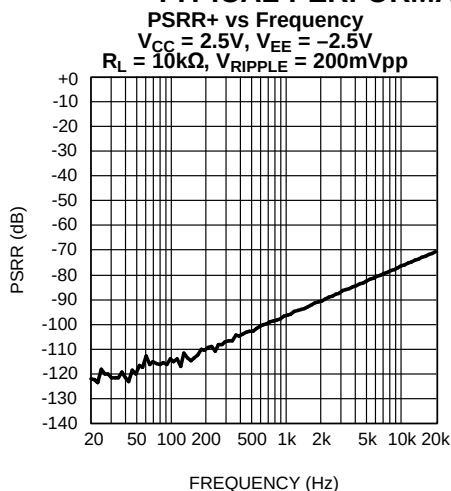
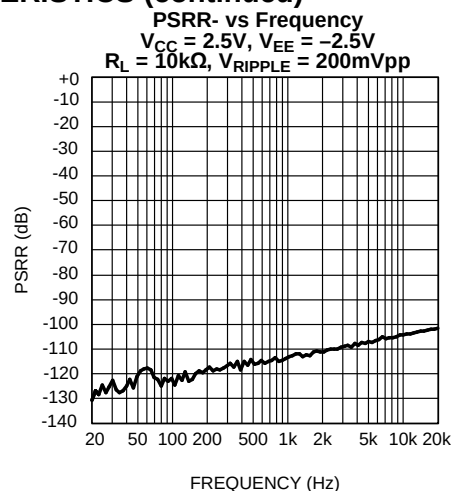
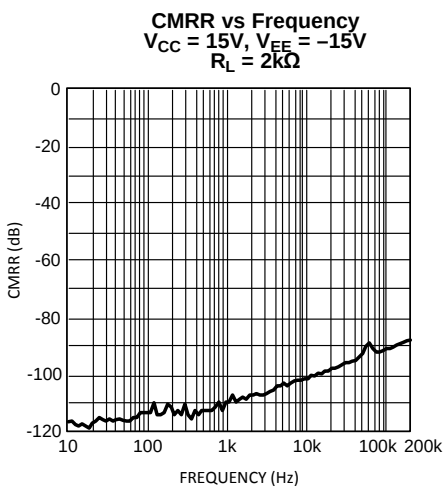
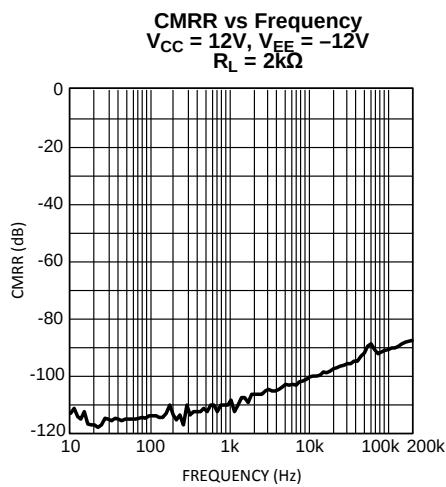
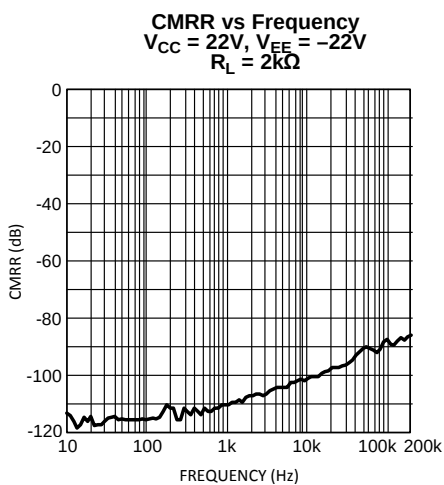
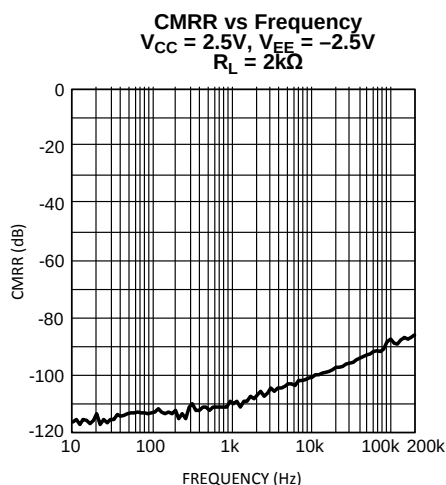


Figure 80.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 81.****Figure 82.****Figure 83.****Figure 84.****Figure 85.****Figure 86.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

CMRR vs Frequency
 $V_{CC} = 15V$, $V_{EE} = -15V$
 $R_L = 600\Omega$

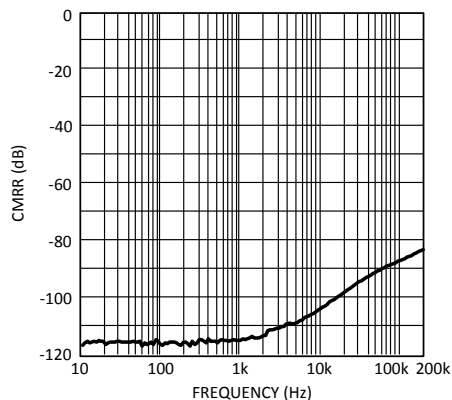


Figure 87.

CMRR vs Frequency
 $V_{CC} = 12V$, $V_{EE} = -12V$
 $R_L = 600\Omega$

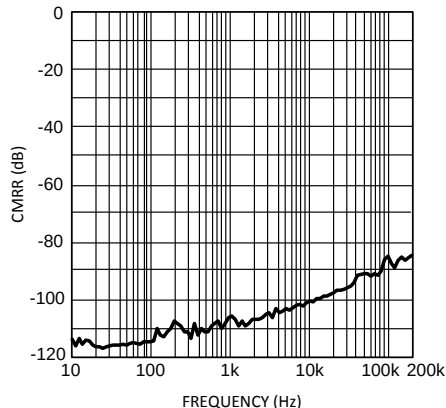


Figure 88.

CMRR vs Frequency
 $V_{CC} = 22V$, $V_{EE} = -22V$
 $R_L = 600\Omega$

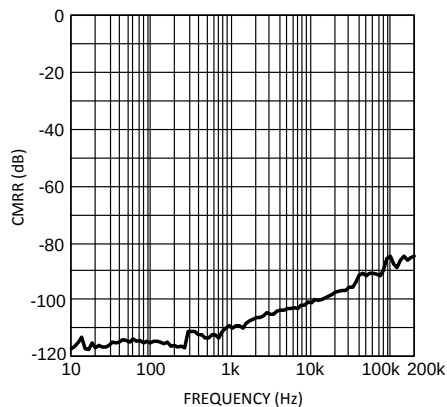


Figure 89.

CMRR vs Frequency
 $V_{CC} = 2.5V$, $V_{EE} = -2.5V$
 $R_L = 600\Omega$

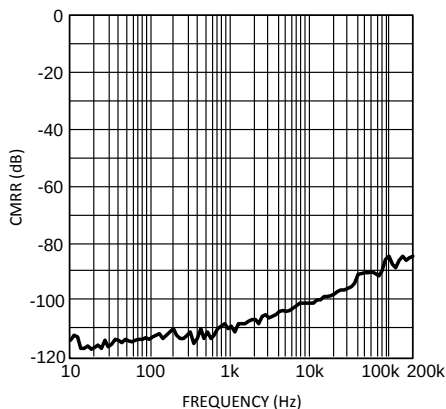


Figure 90.

CMRR vs Frequency
 $V_{CC} = 15V$, $V_{EE} = -15V$
 $R_L = 10k\Omega$

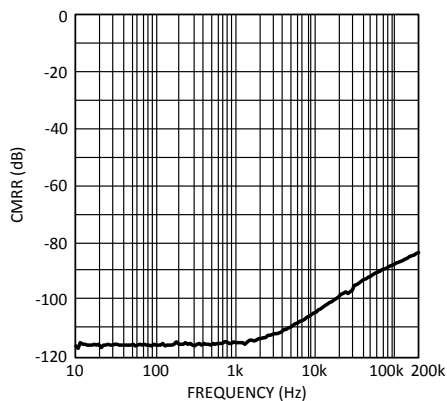


Figure 91.

CMRR vs Frequency
 $V_{CC} = 12V$, $V_{EE} = -12V$
 $R_L = 10k\Omega$

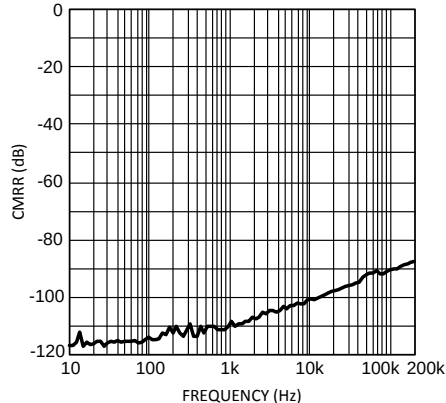
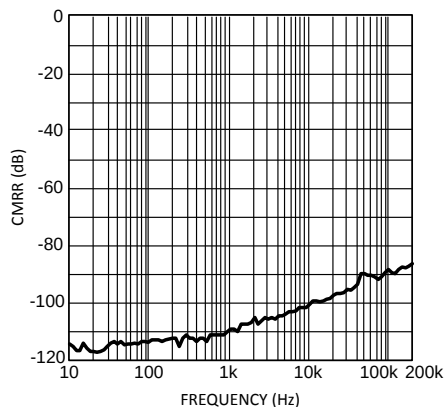


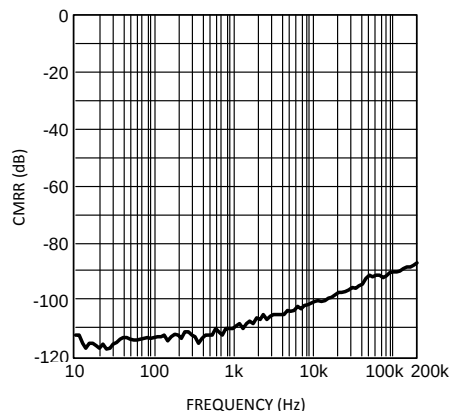
Figure 92.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

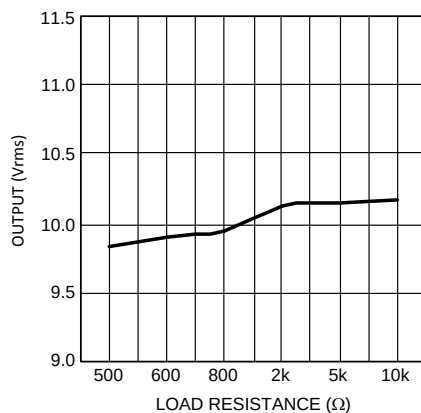
CMRR vs Frequency
 $V_{CC} = 22V$, $V_{EE} = -22V$
 $R_L = 10k\Omega$

**Figure 93.**

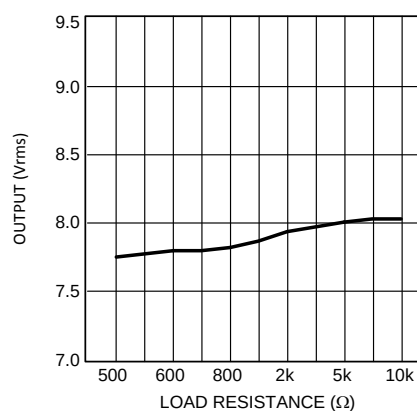
CMRR vs Frequency
 $V_{CC} = 2.5V$, $V_{EE} = -2.5V$
 $R_L = 10k\Omega$

**Figure 94.**

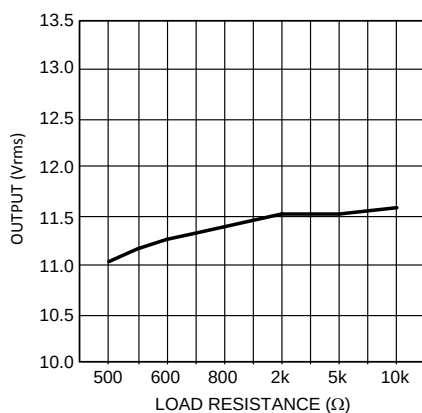
Output Voltage vs Load Resistance
 $V_{CC} = 15V$, $V_{EE} = -15V$
 $THD+N = 1\%$

**Figure 95.**

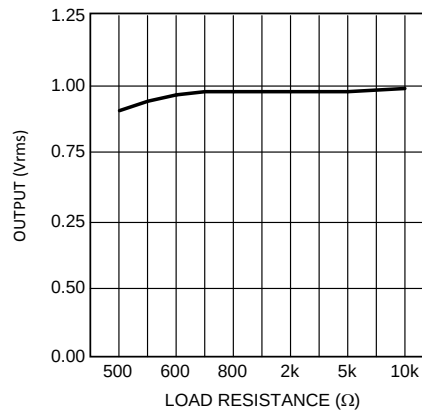
Output Voltage vs Load Resistance
 $V_{CC} = 12V$, $V_{EE} = -12V$
 $THD+N = 1\%$

**Figure 96.**

Output Voltage vs Load Resistance
 $V_{CC} = 22V$, $V_{EE} = -22V$
 $THD+N = 1\%$

**Figure 97.**

Output Voltage vs Load Resistance
 $V_{CC} = 2.5V$, $V_{EE} = -2.5V$
 $THD+N = 1\%$

**Figure 98.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Voltage vs Total Power Supply Voltage
 $R_L = 2k\Omega$, THD+N = 1%

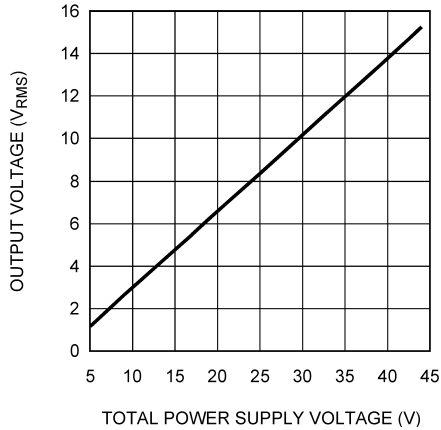


Figure 99.

Output Voltage vs Total Power Supply Voltage
 $R_L = 600\Omega$, THD+N = 1%

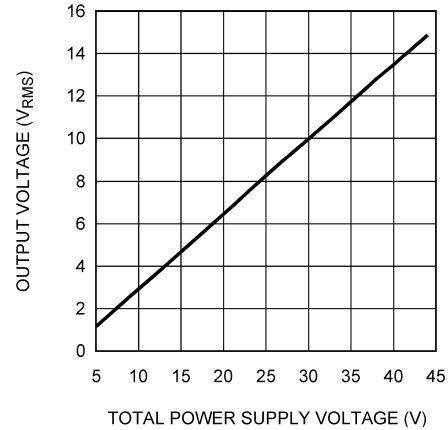


Figure 100.

Output Voltage vs Total Power Supply Voltage
 $R_L = 10k\Omega$, THD+N = 1%

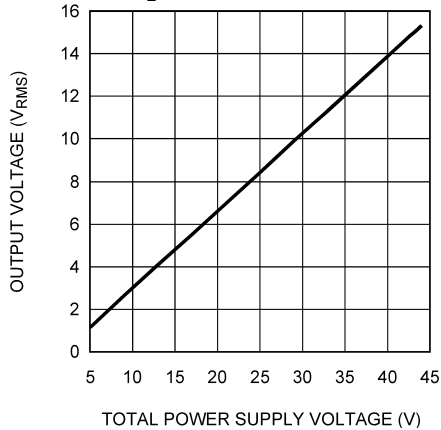


Figure 101.

Power Supply Current vs Total Power Supply Voltage
 $R_L = 2k\Omega$

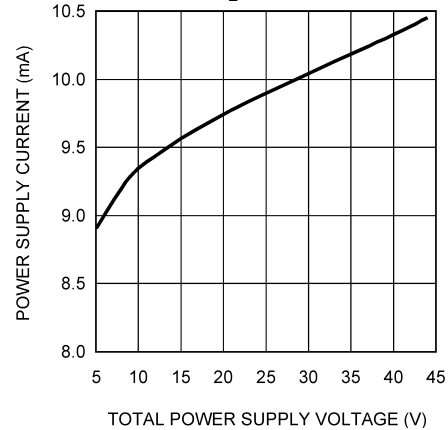


Figure 102.

Power Supply Current vs Total Power Supply Voltage
 $R_L = 600\Omega$

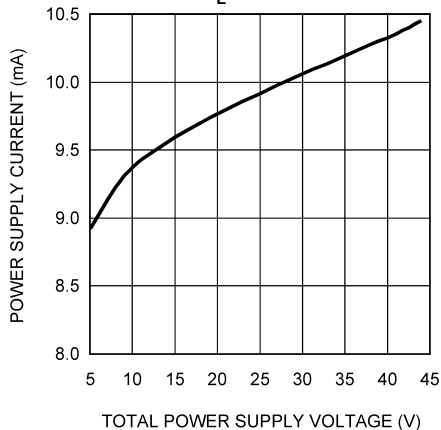


Figure 103.

Power Supply Current vs Total Power Supply Voltage
 $R_L = 10k\Omega$

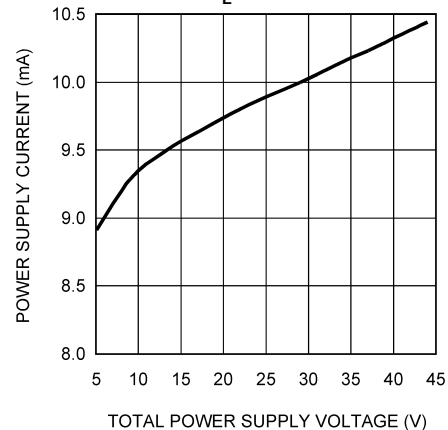


Figure 104.

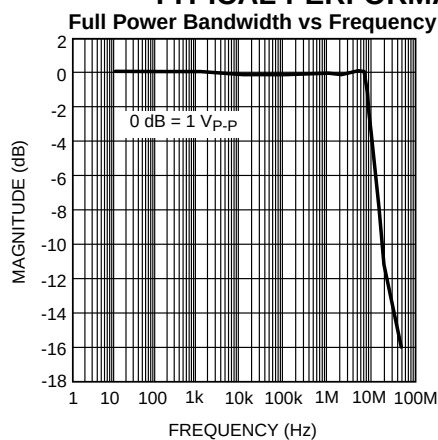
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 105.

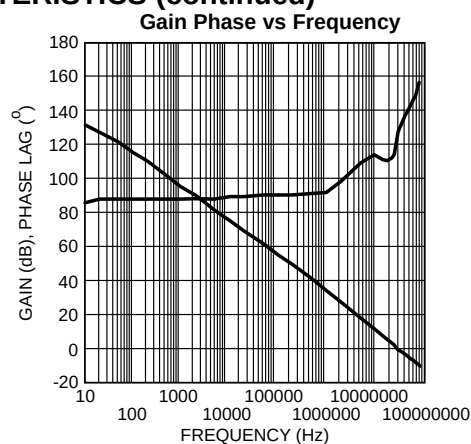


Figure 106.

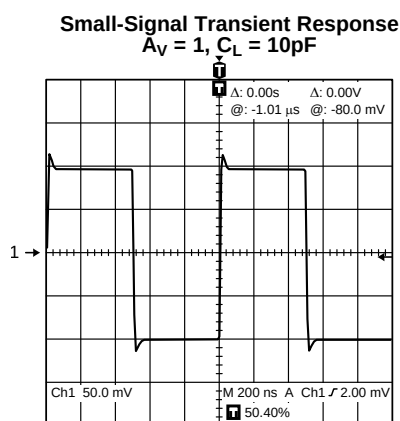


Figure 107.

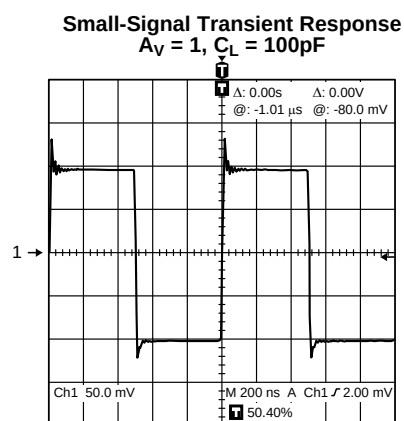


Figure 108.

APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49860 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49860's low residual distortion is an input referred internal error. As shown in Figure 109, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 109.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

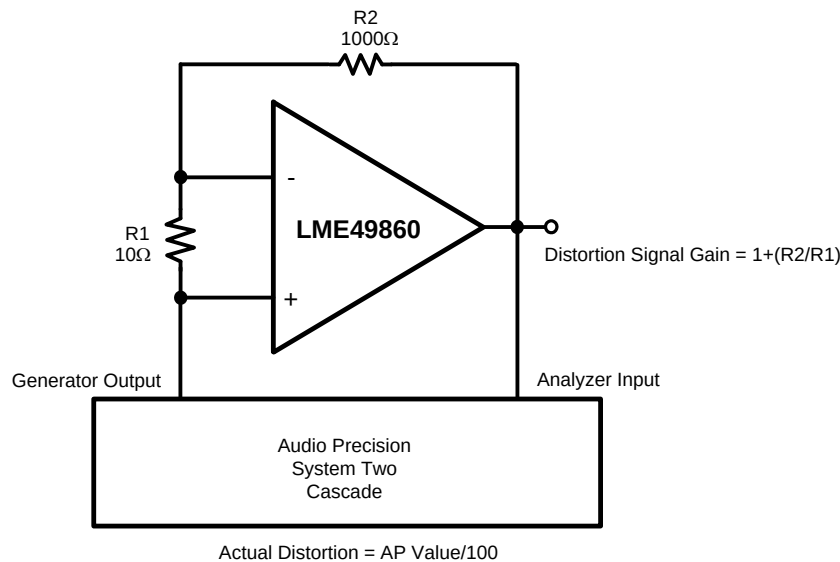
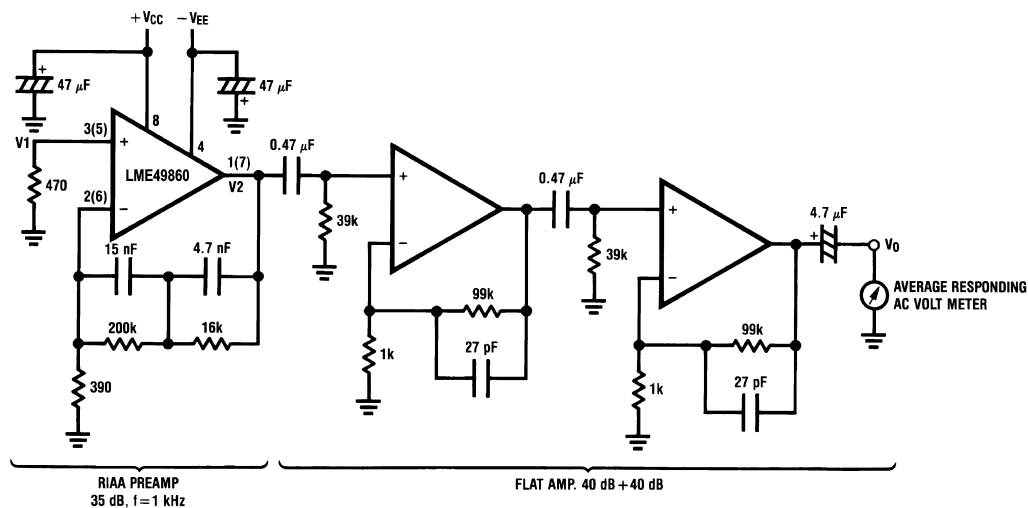


Figure 109. THD+N and IMD Distortion Test Circuit

The LME49860 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.



Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

Figure 110. Noise Measurement Circuit
Total Gain: 115 dB @ $f = 1$ kHz
Input Referred Noise Voltage: $e_n = V_0/560,000$ (V)

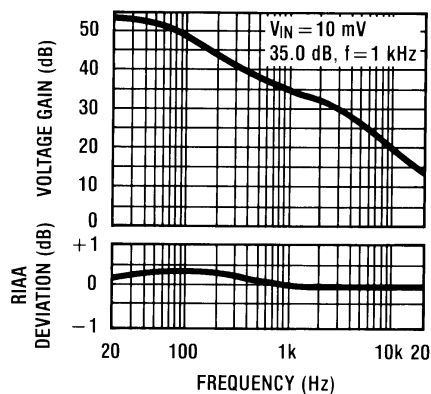


Figure 111. RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency

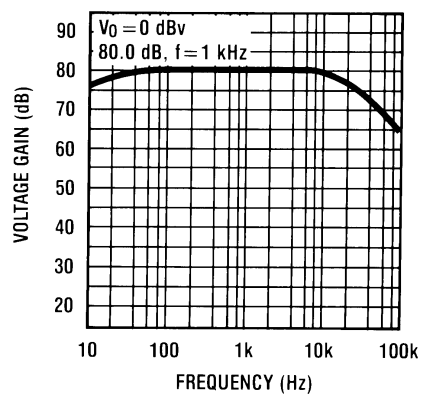
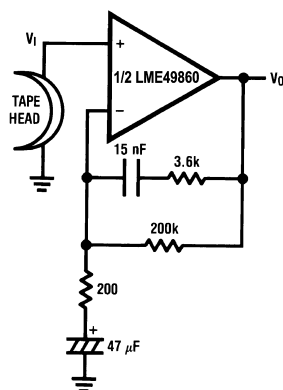


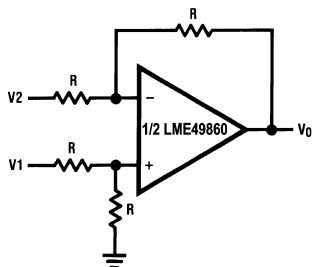
Figure 112. Flat Amp Voltage Gain vs Frequency

TYPICAL APPLICATIONS



$A_V = 34.5$
 $F = 1 \text{ kHz}$
 $E_n = 0.38 \mu\text{V}$
 A Weighted

Figure 113. NAB Preamp



$$V_O = V1 - V2$$

Figure 115. Balanced to Single Ended Converter

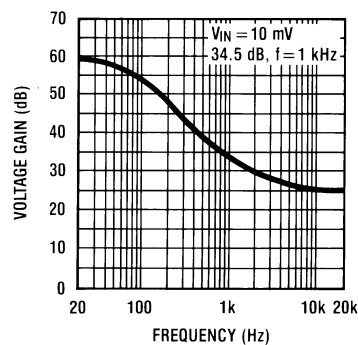
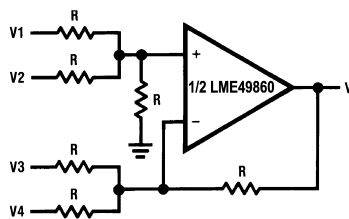
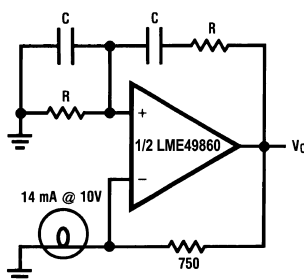


Figure 114. NAB Preamp Voltage Gain vs Frequency



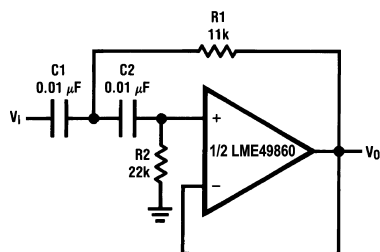
$$V_O = V1 + V2 - V3 - V4$$

Figure 116. Adder/Subtractor



$$f_o = \frac{1}{2\pi RC}$$

Figure 117. Sine Wave Oscillator



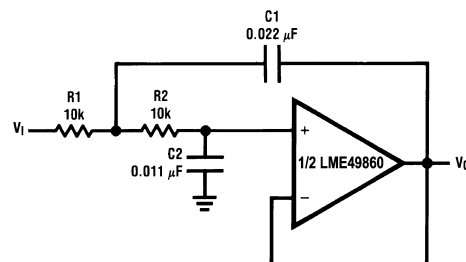
if $C_1 = C_2 = C$

$$R_1 = \frac{\sqrt{2}}{2\omega_0 C}$$

$$R_2 = 2 \cdot R_1$$

Illustration is $f_0 = 1 \text{ kHz}$

Figure 118. Second Order High Pass Filter (Butterworth)



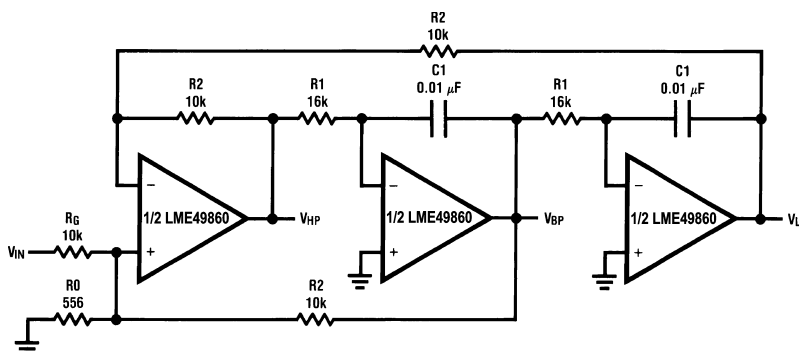
if $R_1 = R_2 = R$

$$C_1 = \frac{\sqrt{2}}{\omega_0 R}$$

$$C_2 = \frac{C_1}{2}$$

Illustration is $f_0 = 1 \text{ kHz}$

Figure 119. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C_1 R_1}, Q = \frac{1}{2} \left(1 + \frac{R_2}{R_0} + \frac{R_2}{R_G} \right), A_{BP} = Q A_{LP} = Q A_{LH} = \frac{R_2}{R_G}$$

Illustration is $f_0 = 1 \text{ kHz}$, $Q = 10$, $A_{BP} = 1$

Figure 120. State Variable Filter

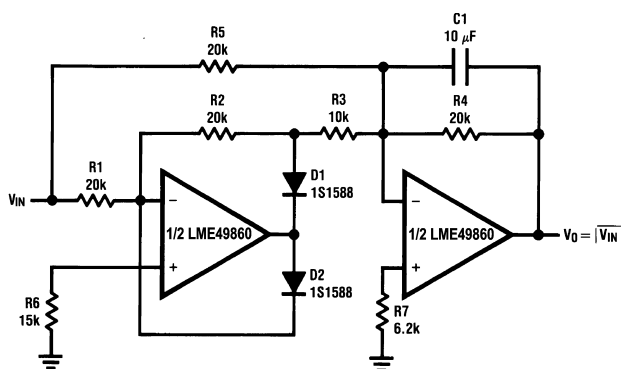


Figure 121. AC/DC Converter

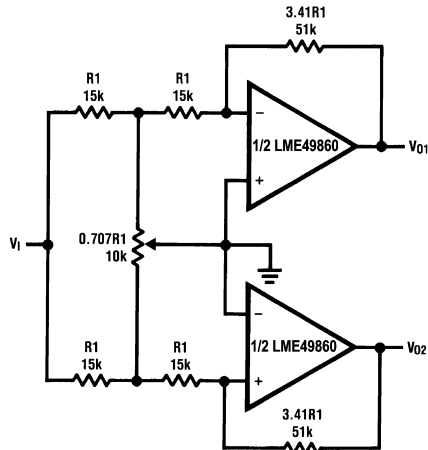


Figure 122. 2 Channel Panning Circuit (Pan Pot)

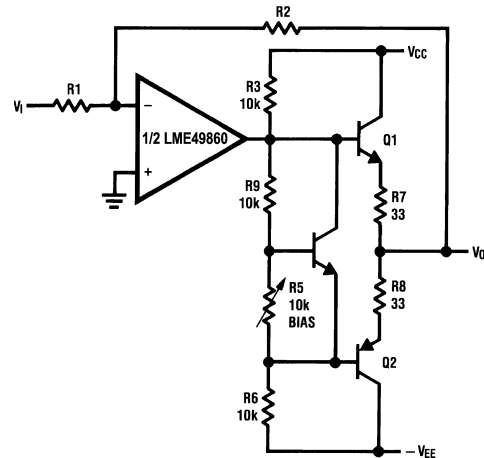
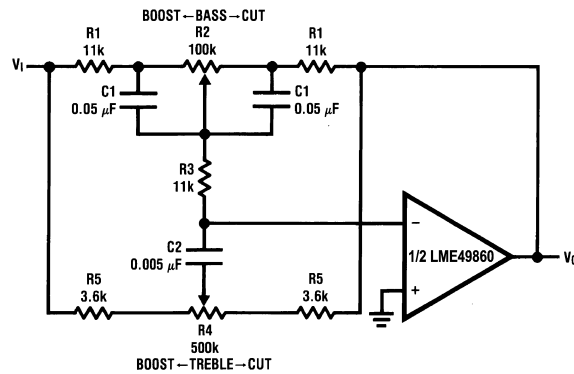


Figure 123. Line Driver



$$f_L = \frac{1}{2\pi R_2 C_1}, f_{LB} = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_5 C_2}, f_{HB} = \frac{1}{2\pi (R_1 + R_5 + 2R_3) C_2}$$

Illustration is:

$$f_L = 32 \text{ Hz}, f_{LB} = 320 \text{ Hz}$$

$$f_H = 11 \text{ kHz}, f_{HB} = 1.1 \text{ kHz}$$

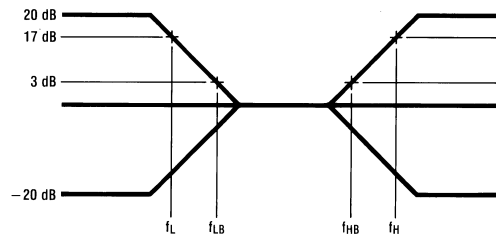
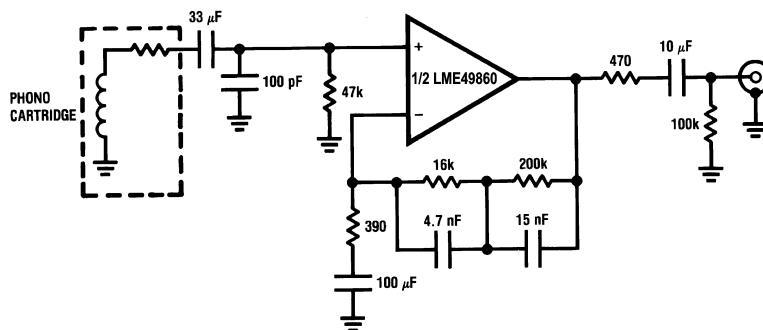
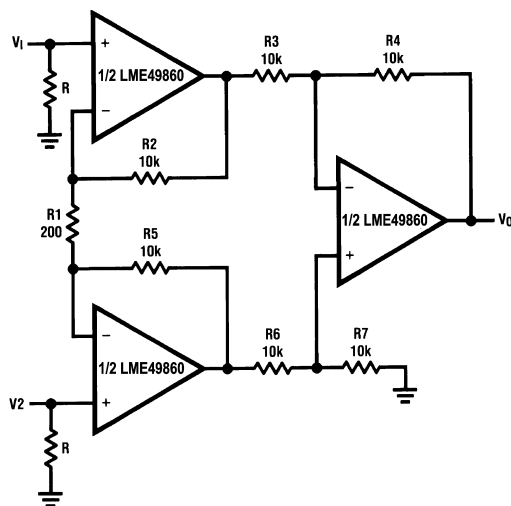


Figure 124. Tone Control



$A_v = 35 \text{ dB}$
 $E_n = 0.33 \mu\text{V}$
 $S/N = 90 \text{ dB}$
 $f = 1 \text{ kHz}$
 $A \text{ Weighted}$
 $A \text{ Weighted, } V_{IN} = 10 \text{ mV}$
 $@f = 1 \text{ kHz}$

Figure 125. RIAA Preamp



If $R_2 = R_5$, $R_3 = R_6$, $R_4 = R_7$

$$V_0 = \left(1 + \frac{2R_2}{R_1}\right) \frac{R_4}{R_3} (V_2 - V_1)$$

Illustration is:

$$V_0 = 101(V_2 - V_1)$$

Figure 126. Balanced Input Mic Amp

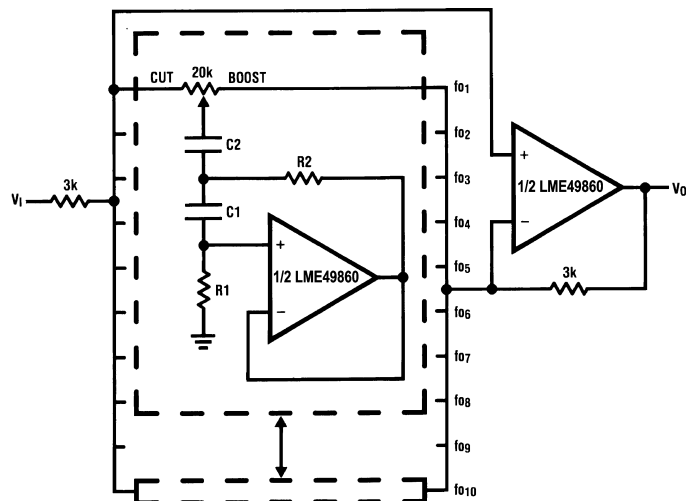


Figure 127. 10 Band Graphic Equalizer

fo (Hz)	C ₁	C ₂	R ₁	R ₂
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

REVISION HISTORY

Rev	Date	Description
1.0	06/01/07	Initial release.
1.1	06/11/07	Added the LME49860MA and LME49860NA Top Mark Information.
C	04/05/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49860MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49860 MA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

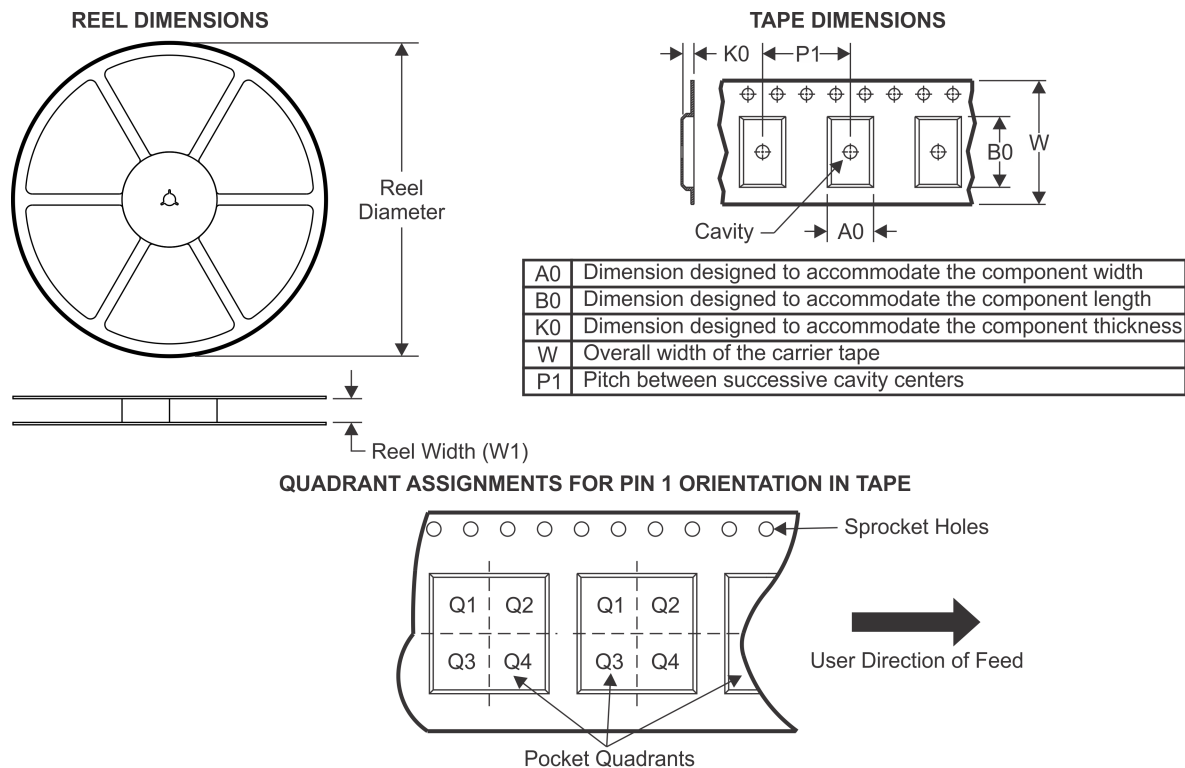
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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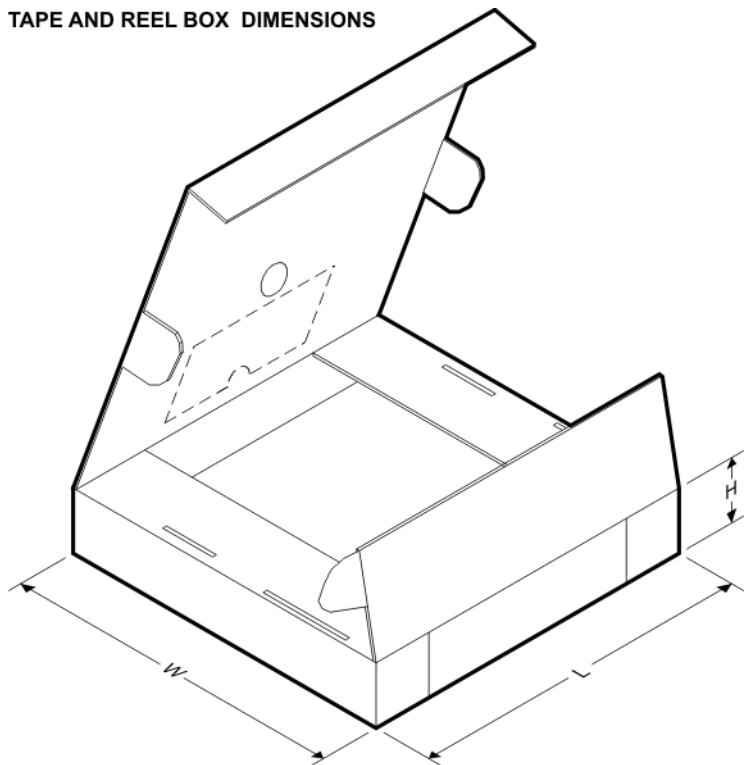
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49860MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

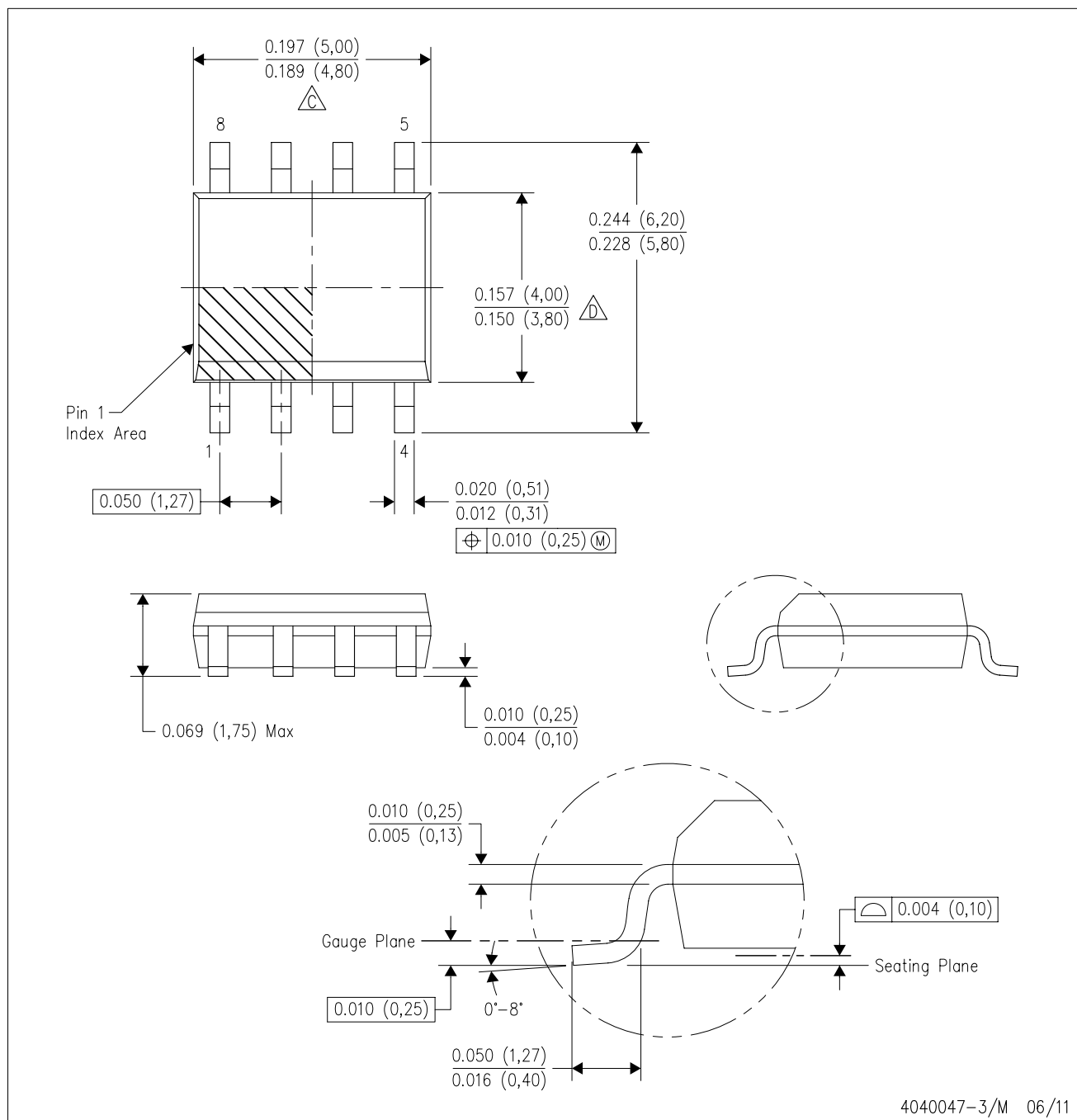


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49860MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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