

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
 - Fully operational to +500V
 - Tolerant to negative transient voltage
 - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
 - Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

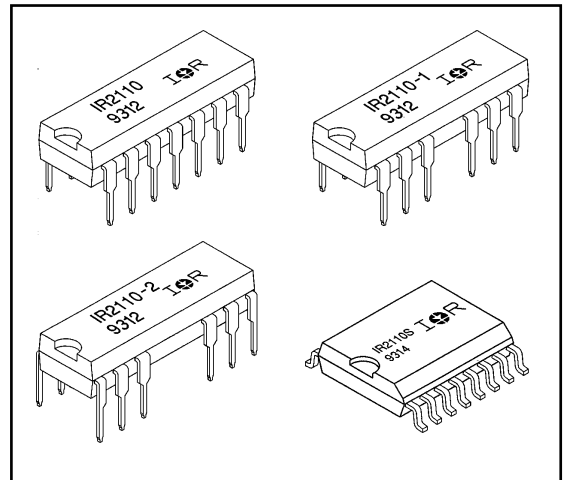
Description

The IR2110 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 volts.

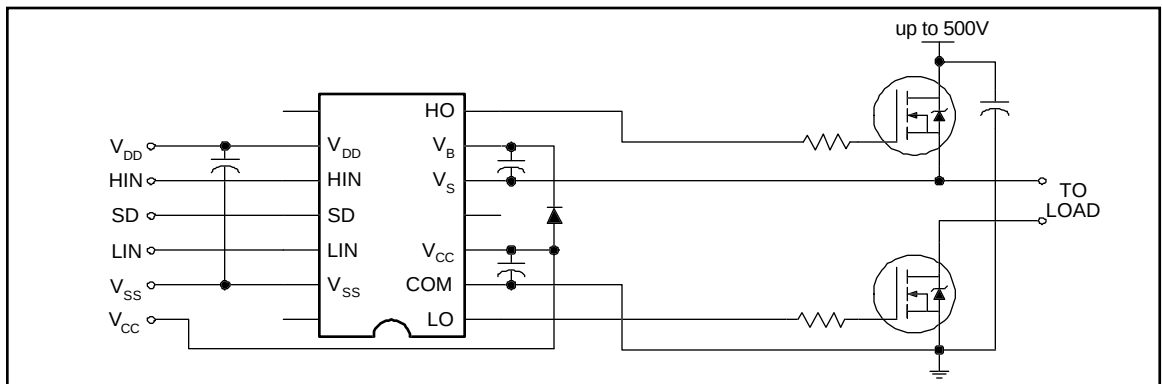
Product Summary

V_{OFFSET}	500V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
t_{on/off} (typ.)	120 & 94 ns
Delay Matching	10 ns

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V_B	High Side Floating Supply Voltage	-0.3	525	V
V_S	High Side Floating Supply Offset Voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{DD}	Logic Supply Voltage	-0.3	$V_{SS} + 25$	
V_{SS}	Logic Supply Offset Voltage	$V_{CC} - 25$	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
dV/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	—	1.6	
	(16 Lead SOIC)	—	1.25	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	$^\circ\text{C/W}$
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 5 & 6)	—	75	
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V_B	High Side Floating Supply Absolute Voltage	$V_S + 10$	$V_S + 20$	V
V_S	High Side Floating Supply Offset Voltage	Note 1	500	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	$V_{SS} + 5$	$V_{SS} + 20$	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_B$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
t_{on}	Turn-On Propagation Delay	7	—	120	150	ns	$V_S = 0V$
t_{off}	Turn-Off Propagation Delay	8	—	94	125		$V_S = 500V$
t_{sd}	Shutdown Propagation Delay	9	—	110	140		$V_S = 500V$
t_r	Turn-On Rise Time	10	—	25	35		
t_f	Turn-Off Fall Time	11	—	17	25		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	10		Figure 5

Static Electrical Characteristics

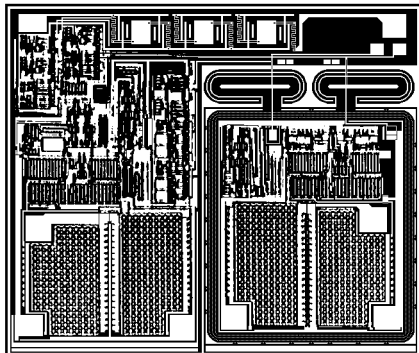
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	14	—	—	1.2		$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	15	—	—	0.1		$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	16	—	—	50	μA	$V_B = V_S = 500V$
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	125	230		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	180	340		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	15	30		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.0	8.2	9.4		
I_{O+}	Output High Short Circuit Pulsed Current	26	2.0	2.5	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	27	2.0	2.5	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

Lead	
Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

14 Lead DIP IR2110	14 Lead DIP w/o Lead 4 IR2110-1	16 Lead DIP w/o Leads 4 & 5 IR2110-2	16 Lead SOIC (Wide Body) IR2110S
Part Number			

Device Information

Process & Design Rule		HVDCMOS 4.0 μm	
Transistor Count		220	
Die Size		100 X 117 X 26 (mil)	
Die Outline			
Thickness of Gate Oxide		800Å	
Connections	First Layer	Material	Poly Silicon
		Width	4 μm
		Spacing	6 μm
		Thickness	5000Å
	Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)
		Width	6 μm
		Spacing	9 μm
		Thickness	20,000Å
Contact Hole Dimension		8 μm X 8 μm	
Insulation Layer	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Passivation (1)	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Passivation (2)	Material	Proprietary*	
	Thickness	Proprietary*	
Method of Saw		Full Cut	
Method of Die Bond		Ablebond 84 - 1	
Wire Bond	Method	Thermo Sonic	
	Material	Au (1.0 mil / 1.3 mil)	
Leadframe	Material	Cu	
	Die Area	Ag	
	Lead Plating	Pb : Sn (37 : 63)	
Package	Types	14 & 16 Lead PDIP / 16 Lead SOIC	
	Materials	EME6300 / MP150 / MP190	
Remarks: * Patent Pending			

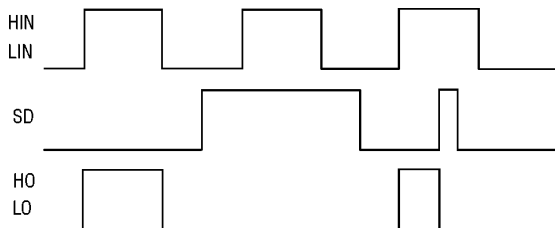


Figure 1. Input/Output Timing Diagram

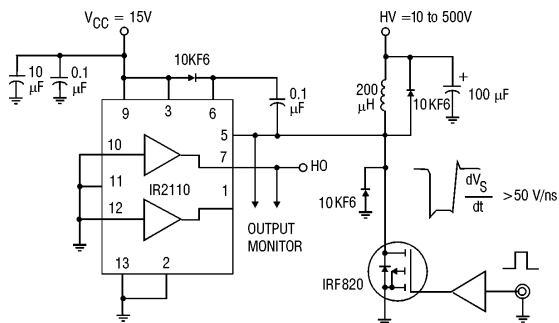


Figure 2. Floating Supply Voltage Transient Test Circuit

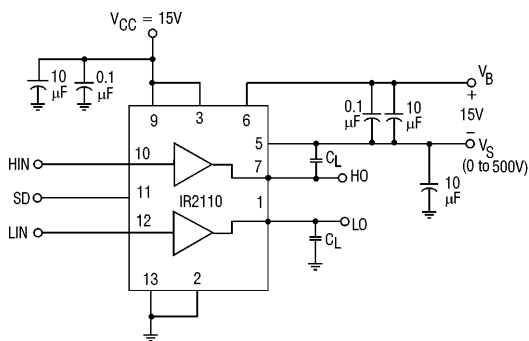


Figure 3. Switching Time Test Circuit

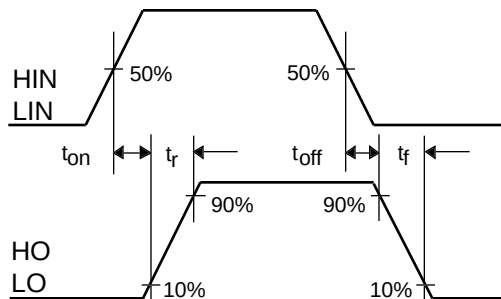


Figure 4. Switching Time Waveform Definition

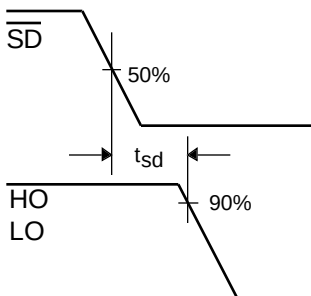


Figure 3. Shutdown Waveform Definitions

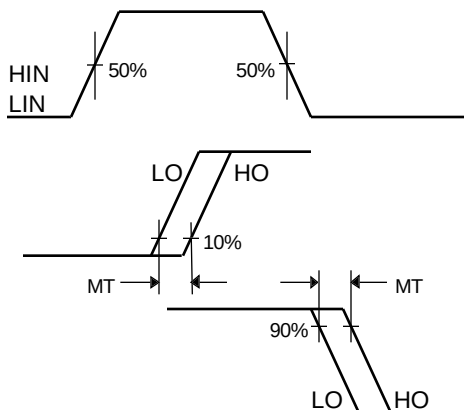


Figure 6. Delay Matching Waveform Definitions

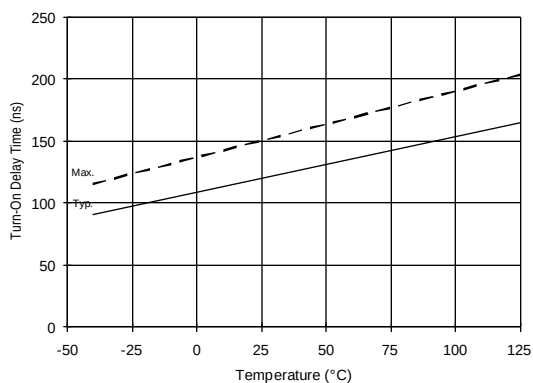


Figure 7A. Turn-On Time vs. Temperature

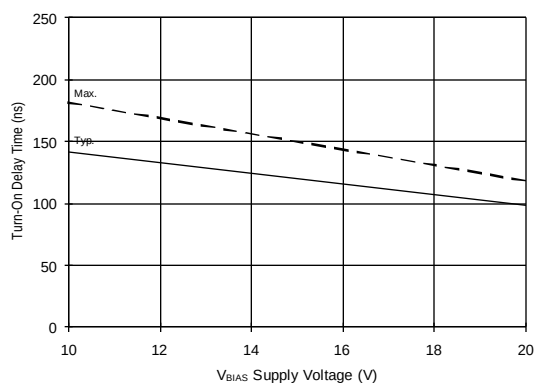


Figure 7B. Turn-On Time vs. Voltage

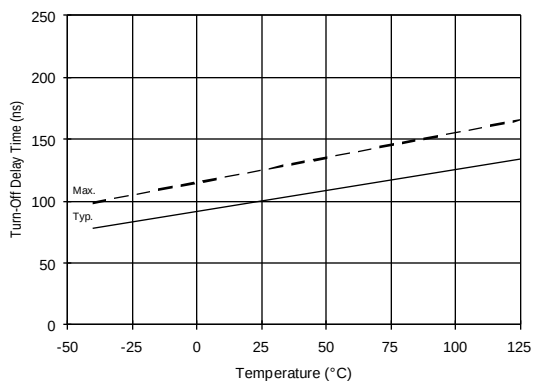


Figure 8A. Turn-Off Time vs. Temperature

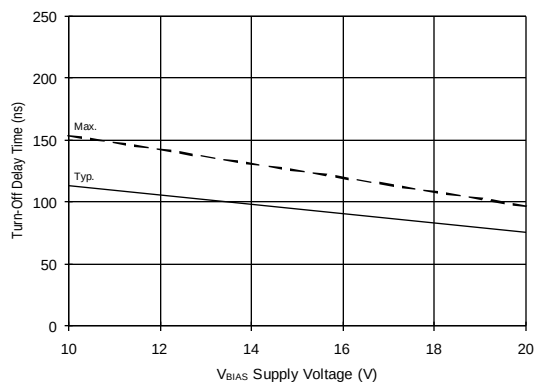


Figure 8B. Turn-Off Time vs. Voltage

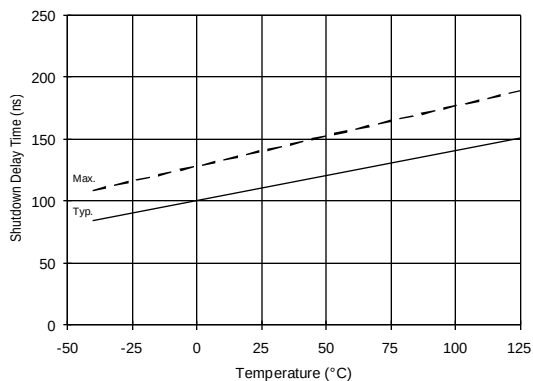


Figure 9A. Shutdown Time vs. Temperature

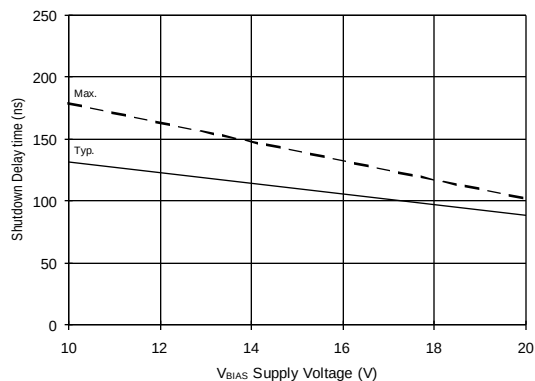


Figure 9B. Shutdown Time vs. Voltage

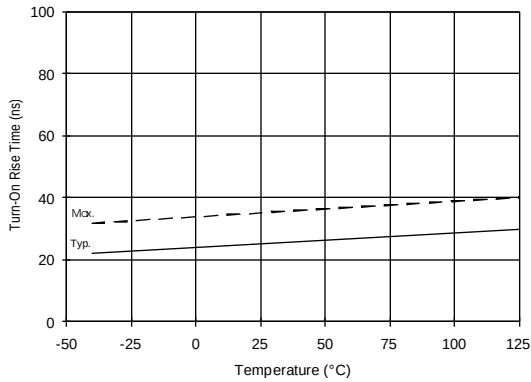


Figure 10A. Turn-On Rise Time vs. Temperature

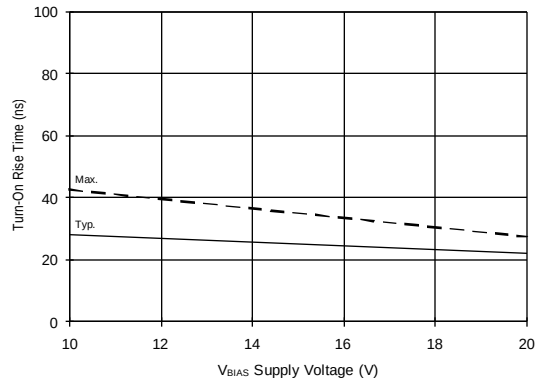


Figure 10B. Turn-On Rise Time vs. Voltage

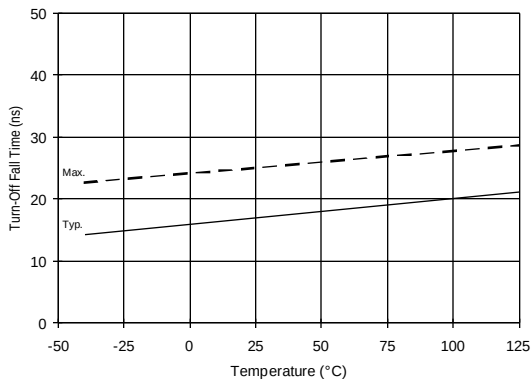


Figure 11A. Turn-Off Fall Time vs. Temperature

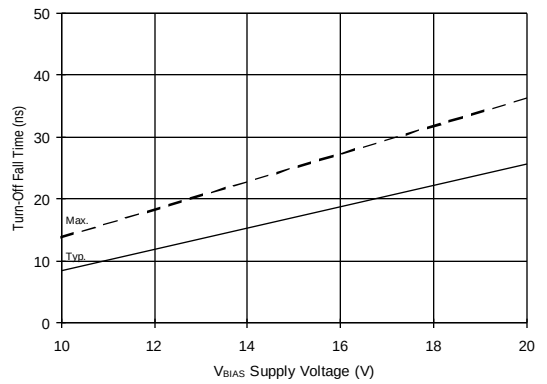


Figure 11B. Turn-Off Fall Time vs. Voltage

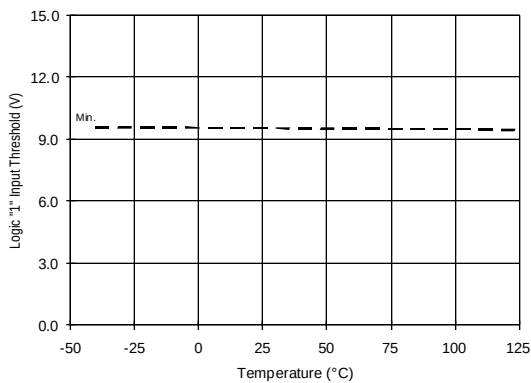


Figure 12A. Logic "1" Input Threshold vs. Temperature

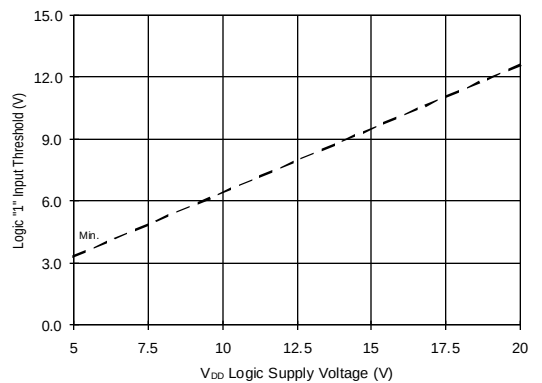


Figure 12B. Logic "1" Input Threshold vs. Voltage

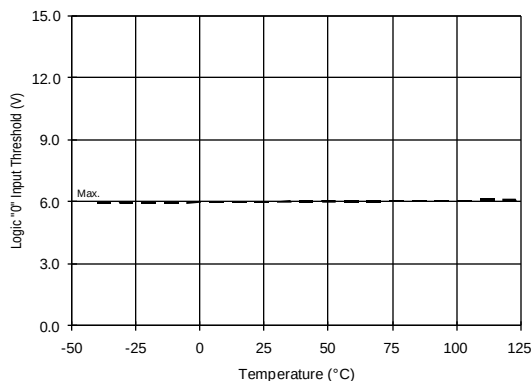


Figure 13A. Logic "0" Input Threshold vs. Temperature

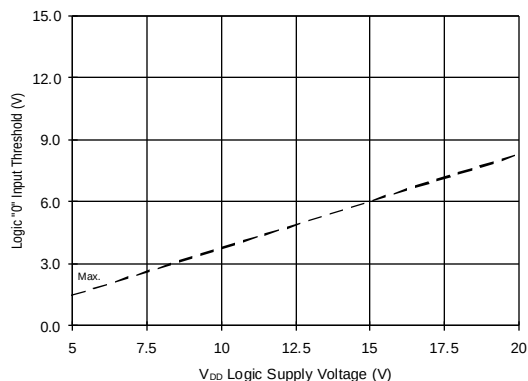


Figure 13B. Logic "0" Input Threshold vs. Voltage

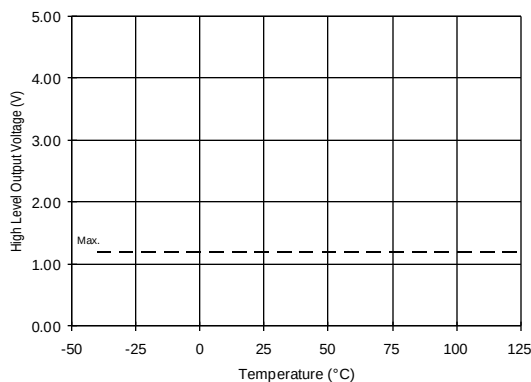


Figure 14A. High Level Output vs. Temperature

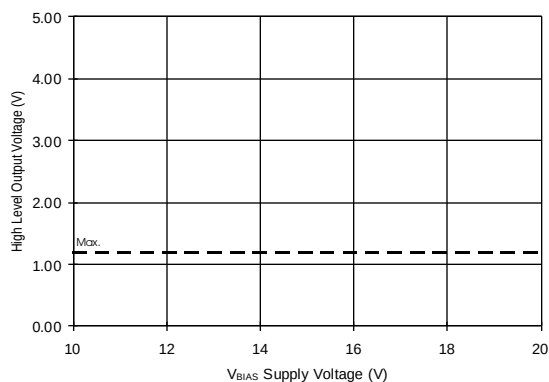


Figure 14B. High Level Output vs. Voltage

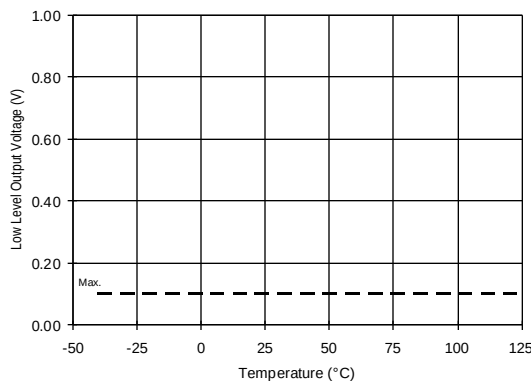


Figure 15A. Low Level Output vs. Temperature

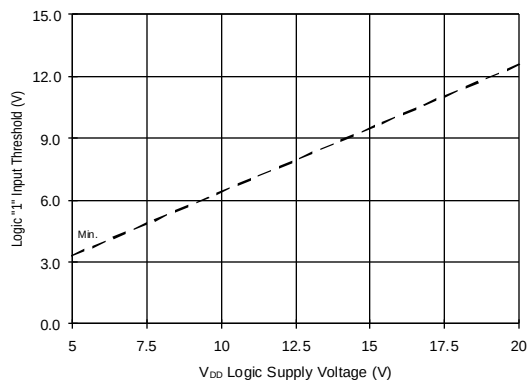


Figure 15B. Low Level Output vs. Voltage

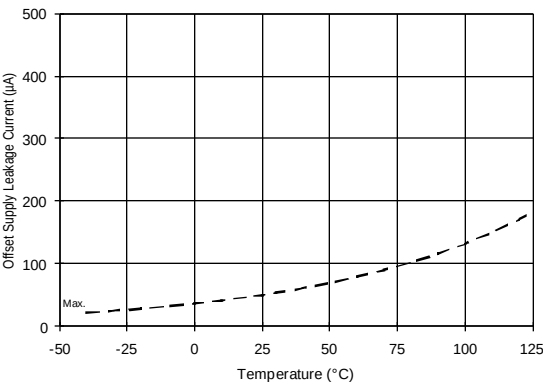


Figure 16A. Offset Supply Current vs. Temperature

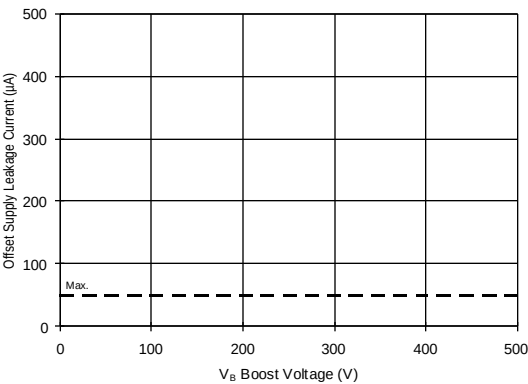


Figure 16B. Offset Supply Current vs. Voltage

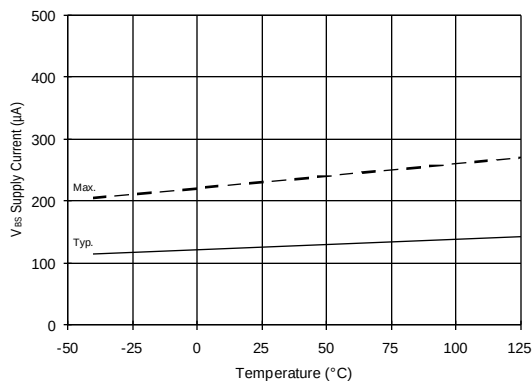


Figure 17A. V_{BS} Supply Current vs. Temperature

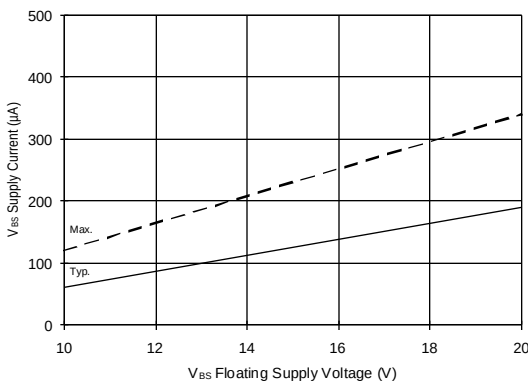


Figure 17B. V_{BS} Supply Current vs. Voltage

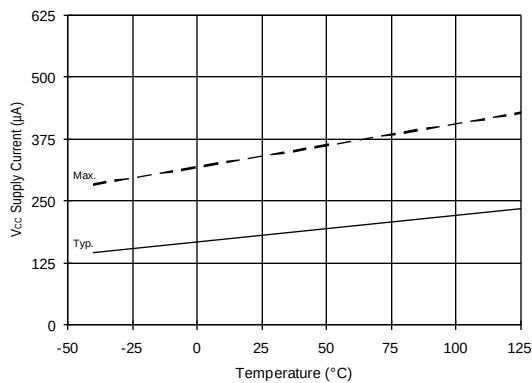


Figure 18A. V_{CC} Supply Current vs. Temperature

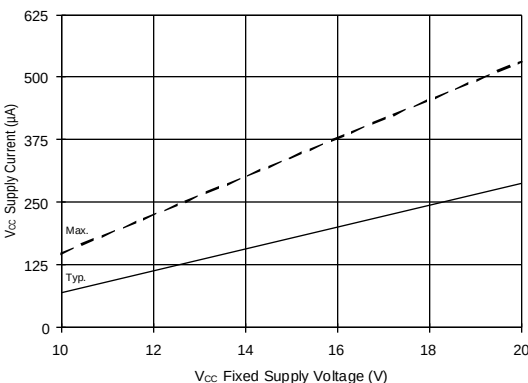


Figure 18B. V_{CC} Supply Current vs. Voltage

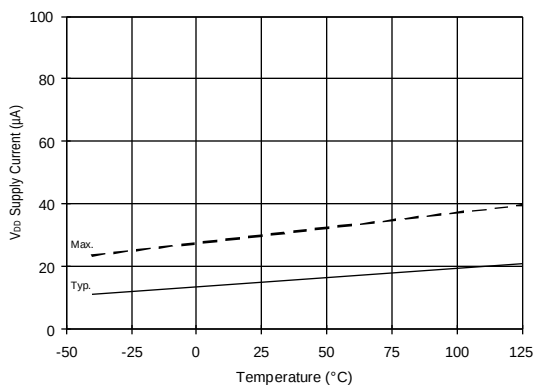


Figure 19A. V_{DD} Supply Current vs. Temperature

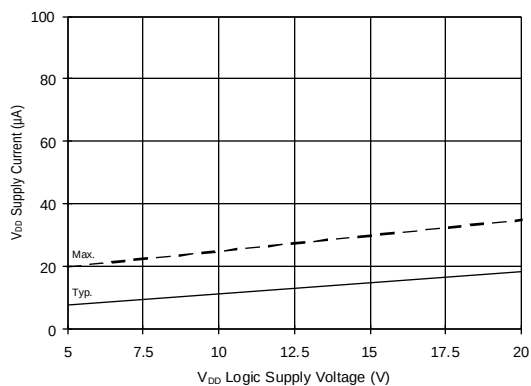


Figure 19B. V_{DD} Supply Current vs. Voltage

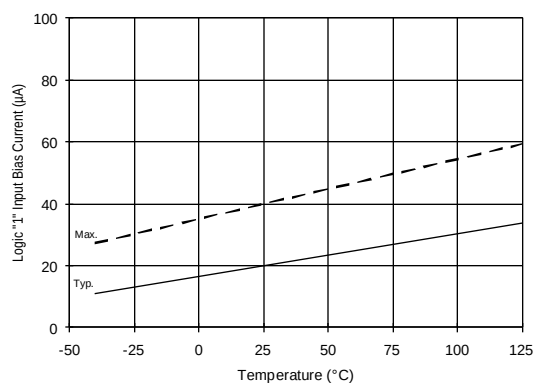


Figure 20A. Logic "1" Input Current vs. Temperature

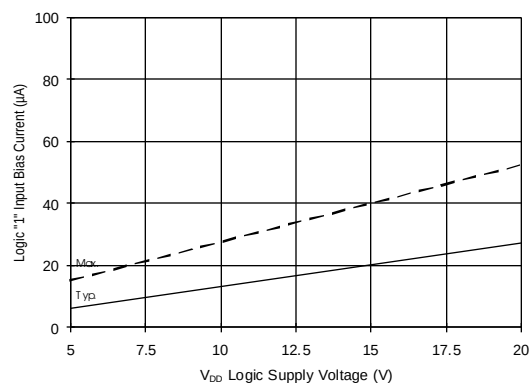


Figure 20B. Logic "1" Input Current vs. Voltage

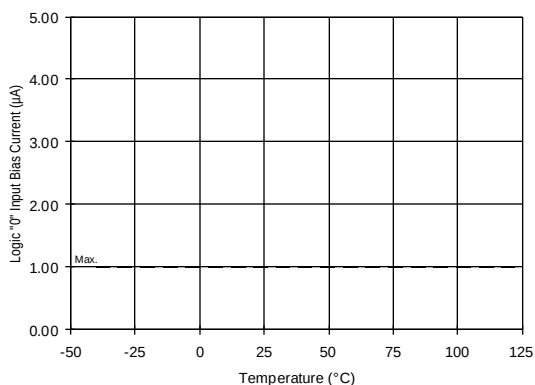


Figure 21A. Logic "0" Input Current vs. Temperature

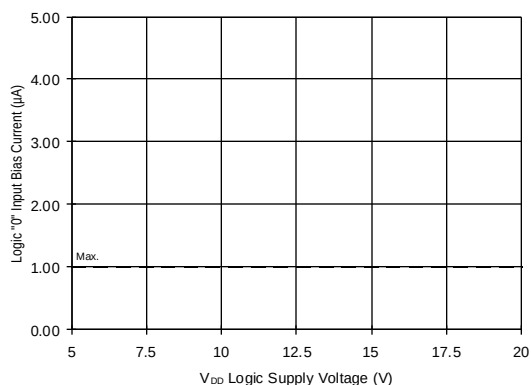


Figure 21B. Logic "0" Input Current vs. Voltage

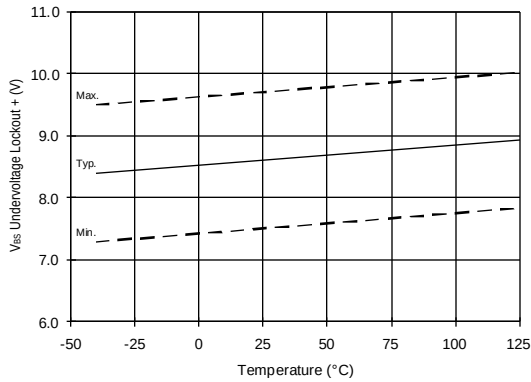


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

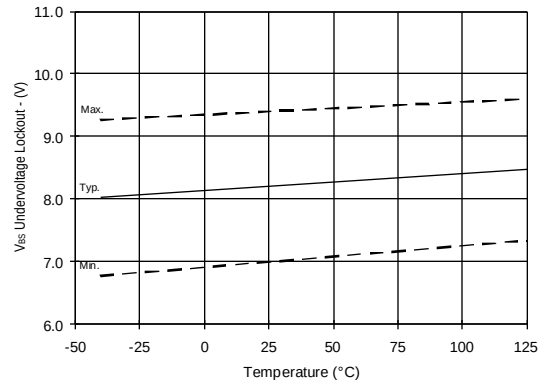


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

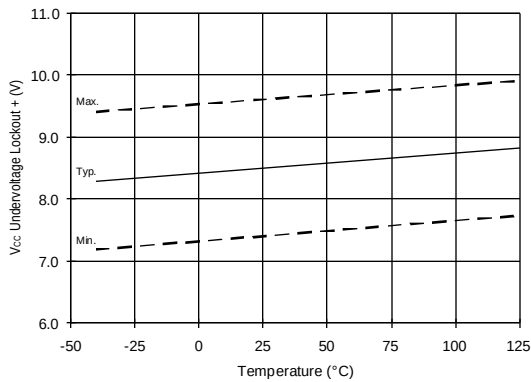


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

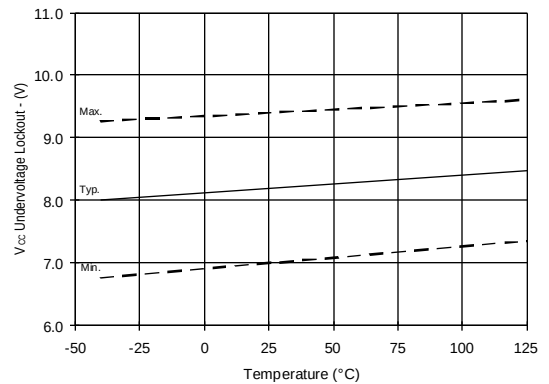


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

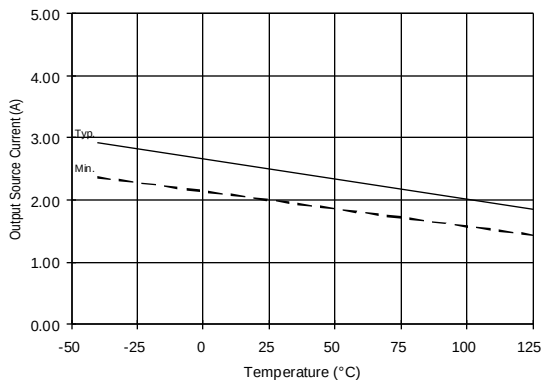


Figure 26A. Output Source Current vs. Temperature

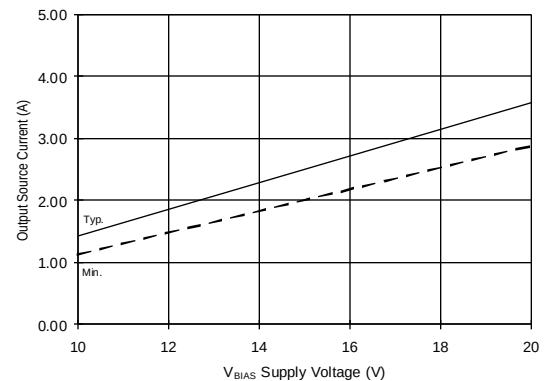


Figure 26B. Output Source Current vs. Voltage

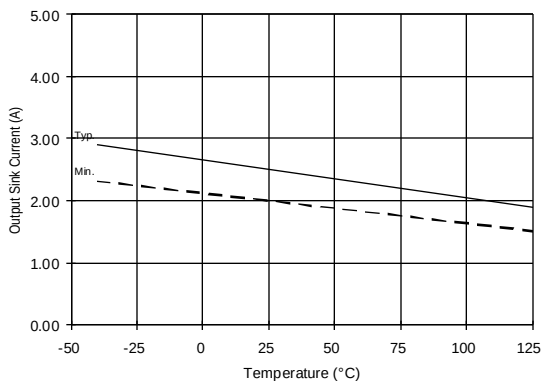


Figure 27A. Output Sink Current vs. Temperature

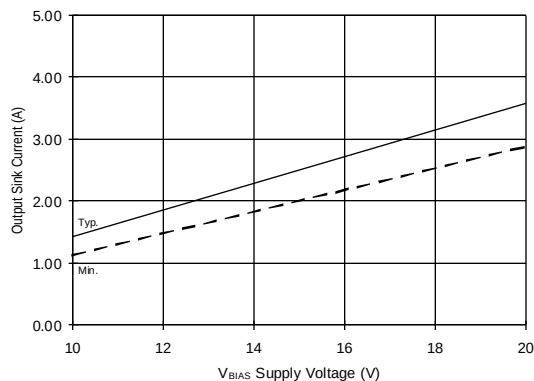


Figure 27B. Output Sink Current vs. Voltage

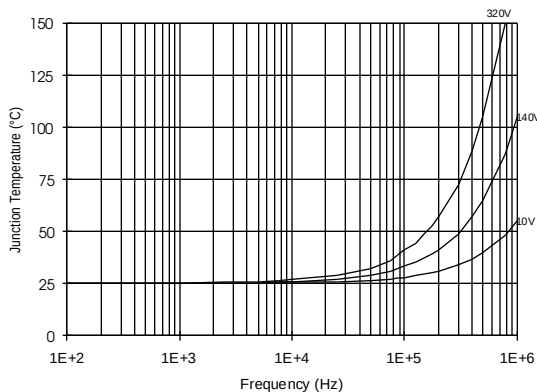


Figure 28. IR2110 T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

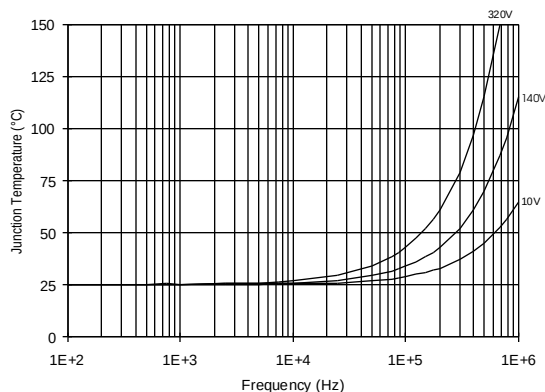


Figure 29. IR2110 T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

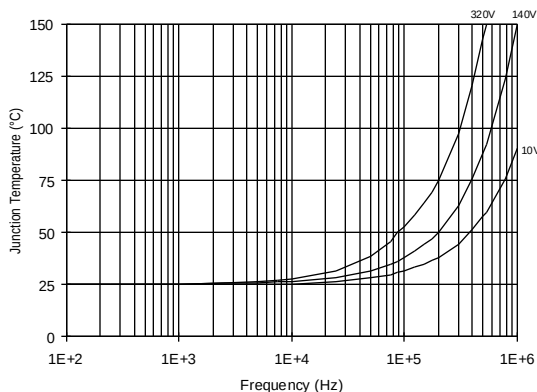


Figure 30. IR2110 T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

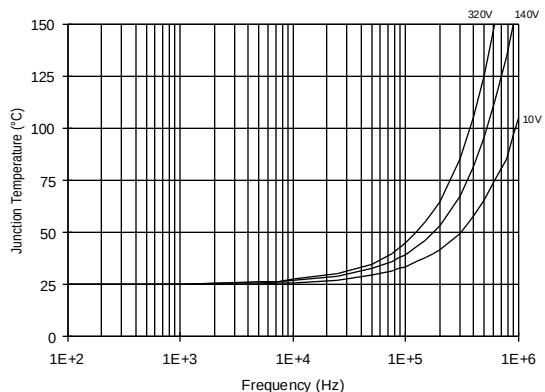


Figure 31. IR2110 T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

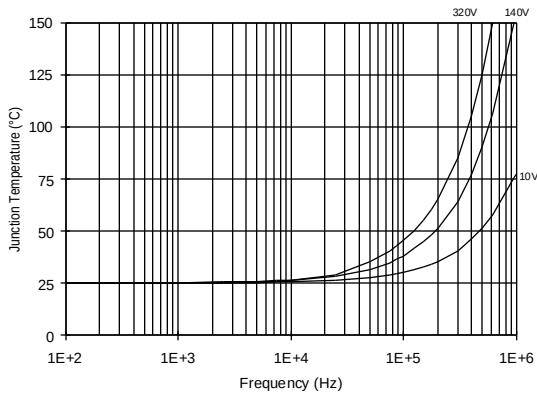


Figure 32. IR2110S T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

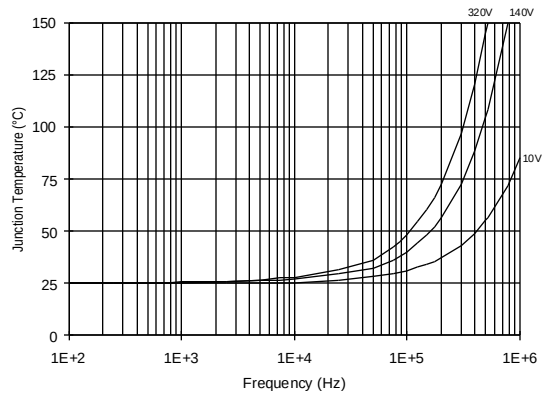


Figure 33. IR2110S T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

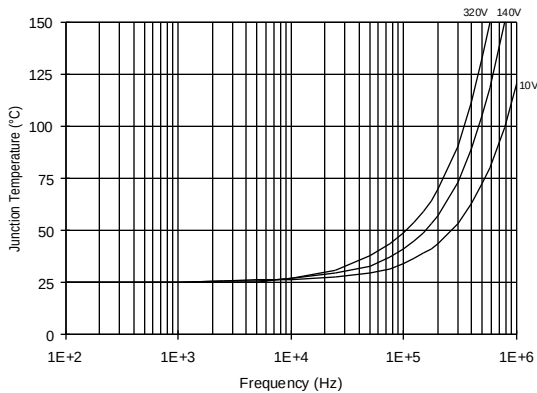


Figure 34. IR2110S T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

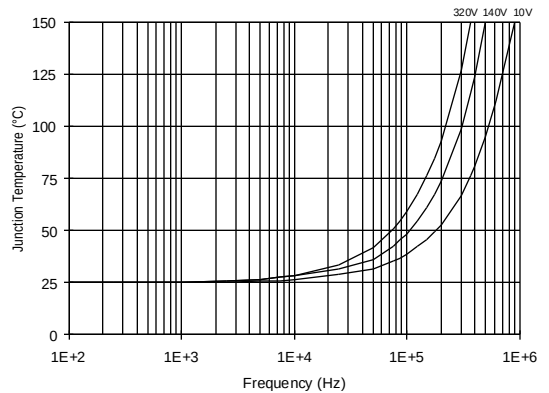


Figure 35. IR2110S T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

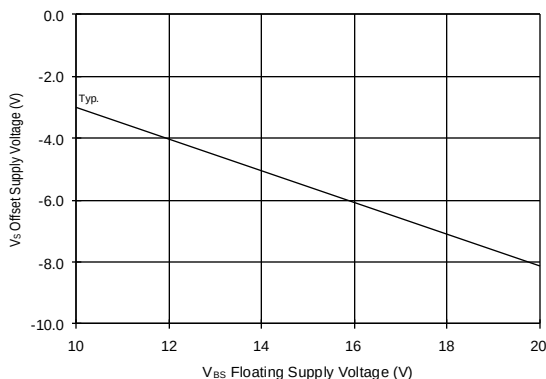


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

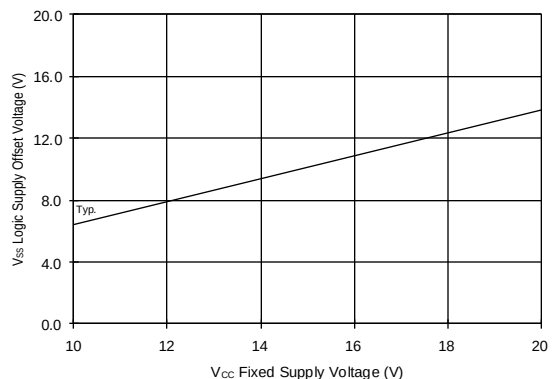


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage