

ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A, HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

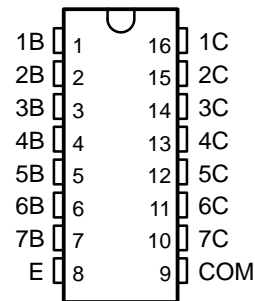
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The ULN2001A is obsolete
and is no longer supplied.

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series
- Package Options Include Plastic Small Outline (D, NS) Packages and Plastic DIP (N)

ULN2001A . . . D OR N PACKAGE
ULN2002A . . . N PACKAGE
ULN2003A, ULN2004A . . . D, N, OR NS PACKAGE
ULQ2003A, ULQ2004A . . . D OR N PACKAGE

(TOP VIEW)



description

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, and ULQ2004A are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULN2003A and ULN2004A, see the SN75468 and SN75469, respectively.

The ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The ULN2003A and ULQ2003A have a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A and ULQ2004A have a 10.5-k Ω series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULN/ULQ2004A is below that of the ULN/ULQ2003A, and the required voltage is less than that required by the ULN2002A.

AVAILABLE OPTIONS

T _A	PACKAGES	
	SMALL OUTLINE (D, NS)	PLASTIC DIP (N)
–20°C to 70°C	–	ULN2002AN
	ULN2003AD ULN2003ANS	ULN2003AN
	ULN2004AD ULN2004ANS	ULN2004AN
–40°C to 85°C	ULQ2003AD	ULQ2003AN
	ULQ2004AD	ULQ2004AN

The D package is available taped and reeled. Add the suffix R to device type (e.g., ULN2003ADR). The NS package is only available taped and reeled.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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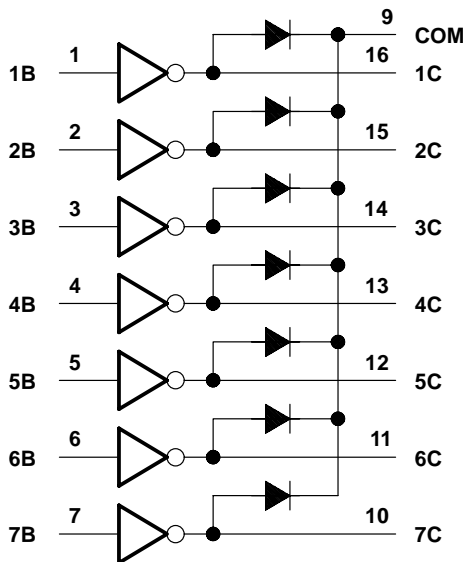
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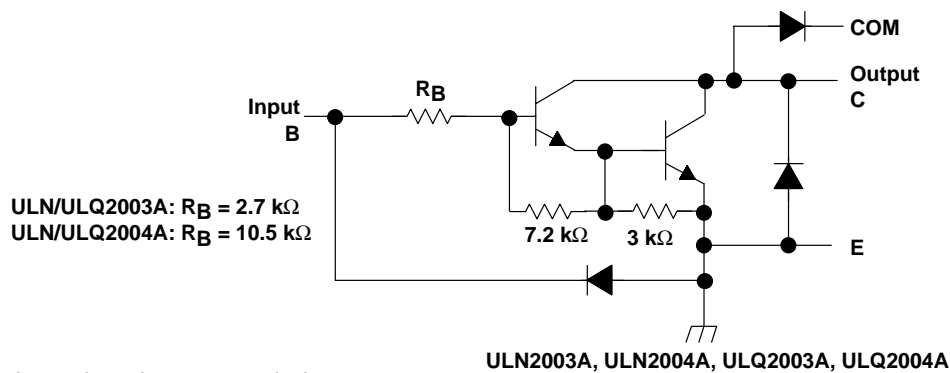
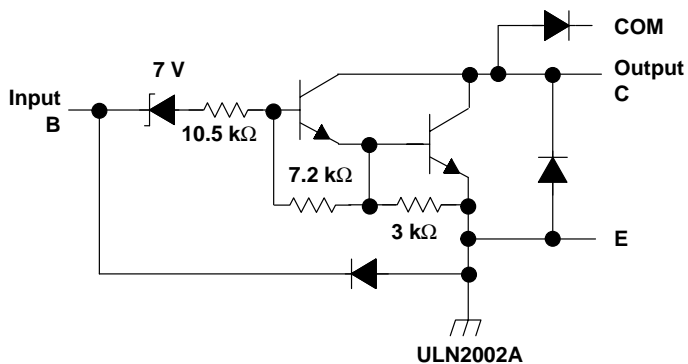
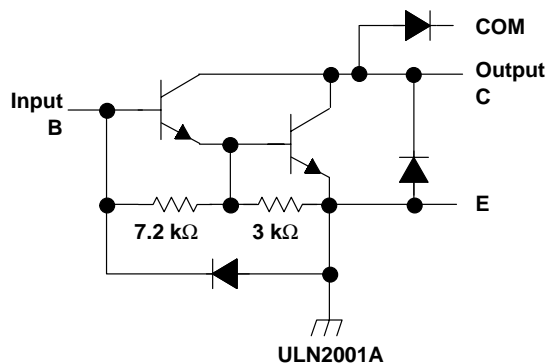
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logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage	50 V
Clamp diode reverse voltage (see Note 1)	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	–2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Operating free-air temperature range, T_A , ULN200xA	–20°C to 70°C
ULQ200xA	–40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	ULN2001A			ULN2002A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	6	$V_{CE} = 2\text{ V}, I_C = 300\text{ mA}$						13	V
$V_{CE(sat)}$ Collector-emitter saturation voltage	5	$I_I = 250\ \mu\text{A}, I_C = 100\text{ mA}$	0.9	1.1		0.9	1.1		V
		$I_I = 350\ \mu\text{A}, I_C = 200\text{ mA}$	1	1.3		1	1.3		
		$I_I = 500\ \mu\text{A}, I_C = 350\text{ mA}$	1.2	1.6		1.2	1.6		
V_F Clamp forward voltage	8	$I_F = 350\text{ mA}$	1.7	2		1.7	2		V
I_{CEX} Collector cutoff current	1	$V_{CE} = 50\text{ V}, I_I = 0$		50			50		μA
	2	$V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}, I_I = 0, V_I = 6\text{ V}$		100			100		
$I_{I(off)}$ Off-state input current	3	$V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}, I_C = 500\ \mu\text{A}$	50	65		50	65		μA
I_I Input current	4	$V_I = 17\text{ V}$				0.82	1.25		mA
I_R Clamp reverse current	7	$V_R = 50\text{ V}, T_A = 70^\circ\text{C}$		100			100		μA
		$V_R = 50\text{ V}$		50			50		
h_{FE} Static forward-current transfer ratio	5	$V_{CE} = 2\text{ V}, I_C = 350\text{ mA}$	1000						
C_i Input capacitance		$V_I = 0, f = 1\text{ MHz}$		15	25		15	25	pF



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electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted) (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$						5	V
			$I_C = 200\text{ mA}$			2.4			6	
			$I_C = 250\text{ mA}$			2.7				
			$I_C = 275\text{ mA}$						7	
			$I_C = 300\text{ mA}$					3		
			$I_C = 350\text{ mA}$						8	
$V_{CE(sat)}$ Collector-emitter saturation voltage	5	$I_I = 250\ \mu\text{A}, I_C = 100\text{ mA}$		0.9	1.1		0.9	1.1	V	
		$I_I = 350\ \mu\text{A}, I_C = 200\text{ mA}$		1	1.3		1	1.3		
		$I_I = 500\ \mu\text{A}, I_C = 350\text{ mA}$		1.2	1.6		1.2	1.6		
I_{CEX} Collector cutoff current	1	$V_{CE} = 50\text{ V}, I_I = 0$						50	μA	
	2	$V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}$	$I_I = 0$					100		
			$V_I = 1\text{ V}$					500		
V_F Clamp forward voltage	8	$I_F = 350\text{ mA}$		1.7	2		1.7	2	V	
$I_{I(off)}$ Off-state input current	3	$V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}$	$I_C = 500\ \mu\text{A}$	50	65		50	65	μA	
I_I Input current	4	$V_I = 3.85\text{ V}$		0.93	1.35				mA	
		$V_I = 5\text{ V}$				0.35	0.5			
		$V_I = 12\text{ V}$				1	1.45			
I_R Clamp reverse current	7	$V_R = 50\text{ V}$			50			50	μA	
		$V_R = 50\text{ V}, T_A = 70^\circ\text{C}$			100			100		
C_i Input capacitance		$V_I = 0,$	$f = 1\text{ MHz}$	15	25		15	25	pF	



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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULQ2003A			ULQ2004A			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
$V_{I(on)}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$						5	V	
			$I_C = 200\text{ mA}$						6		
			$I_C = 250\text{ mA}$								
			$I_C = 275\text{ mA}$								7
			$I_C = 300\text{ mA}$								3
			$I_C = 350\text{ mA}$								
$V_{CE(sat)}$ Collector-emitter saturation voltage	5	$I_I = 250\text{ }\mu\text{A}$, $I_C = 100\text{ mA}$		0.9	1.2		0.9	1.1	V		
		$I_I = 350\text{ }\mu\text{A}$, $I_C = 200\text{ mA}$		1	1.4		1	1.3			
		$I_I = 500\text{ }\mu\text{A}$, $I_C = 350\text{ mA}$		1.2	1.7		1.2	1.6			
I_{CEX} Collector cutoff current	1	$V_{CE} = 50\text{ V}$, $I_I = 0$						100	μA		
	2	$V_{CE} = 50\text{ V}$	$I_I = 0$					100			
			$V_I = 1\text{ V}$					500			
V_F Clamp forward voltage	8	$I_F = 350\text{ mA}$		1.7	2.2		1.7	2	V		
$I_{I(off)}$ Off-state input current	3	$V_{CE} = 50\text{ V}$, $I_C = 500\text{ }\mu\text{A}$		30	65		50	65	μA		
I_I Input current	4	$V_I = 3.85\text{ V}$		0.93	1.35				mA		
		$V_I = 5\text{ V}$					0.35	0.5			
		$V_I = 12\text{ V}$					1	1.45			
I_R Clamp reverse current	7	$V_R = 50\text{ V}$, $T_A = 25^\circ\text{C}$			100			50	μA		
		$V_R = 50\text{ V}$			100			100			
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$		15	25		15	25	pF		

switching characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	ULN2001A, ULN2002A, ULN2003A, ULN2004A			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low- to high-level output	See Figure 9		0.25	1	μs
t_{PHL} Propagation delay time, high- to low-level output	See Figure 9		0.25	1	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$, See Figure 10		$V_S - 20$		mV

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ULQ2003A, ULQ2004A			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low- to high-level output	See Figure 9		1	10	μs
t_{PHL} Propagation delay time, high- to low-level output	See Figure 9		1	10	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$, See Figure 10		$V_S - 500$		mV



PARAMETER MEASUREMENT INFORMATION

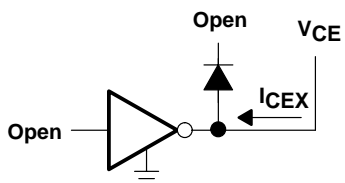


Figure 1. I_{CEX} Test Circuit

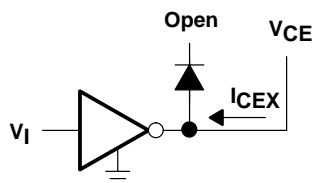


Figure 2. I_{CEX} Test Circuit

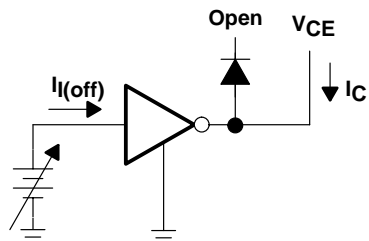


Figure 3. $I_{I(off)}$ Test Circuit

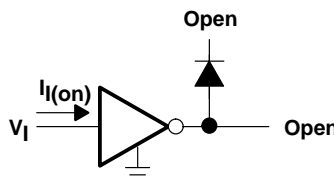
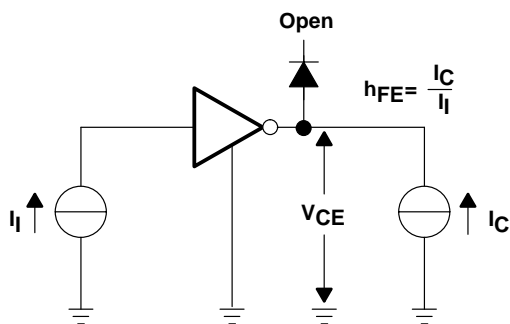


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

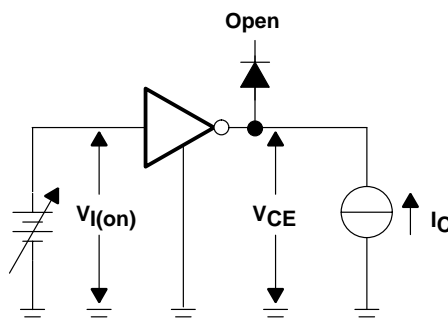


Figure 6. $V_{I(on)}$ Test Circuit

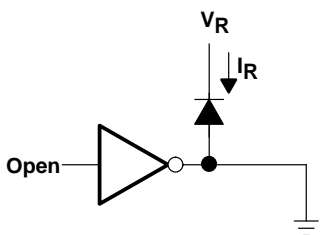


Figure 7. I_R Test Circuit

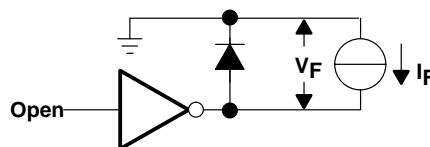


Figure 8. V_F Test Circuit

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PARAMETER MEASUREMENT INFORMATION

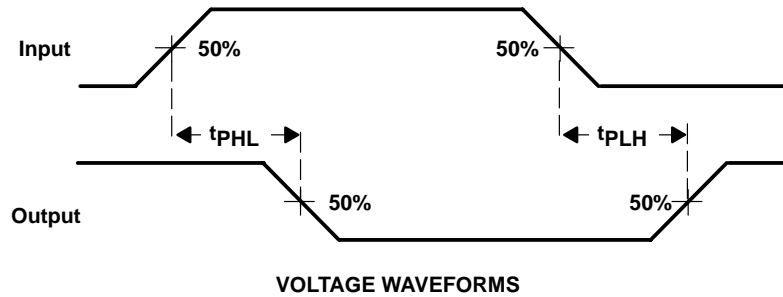
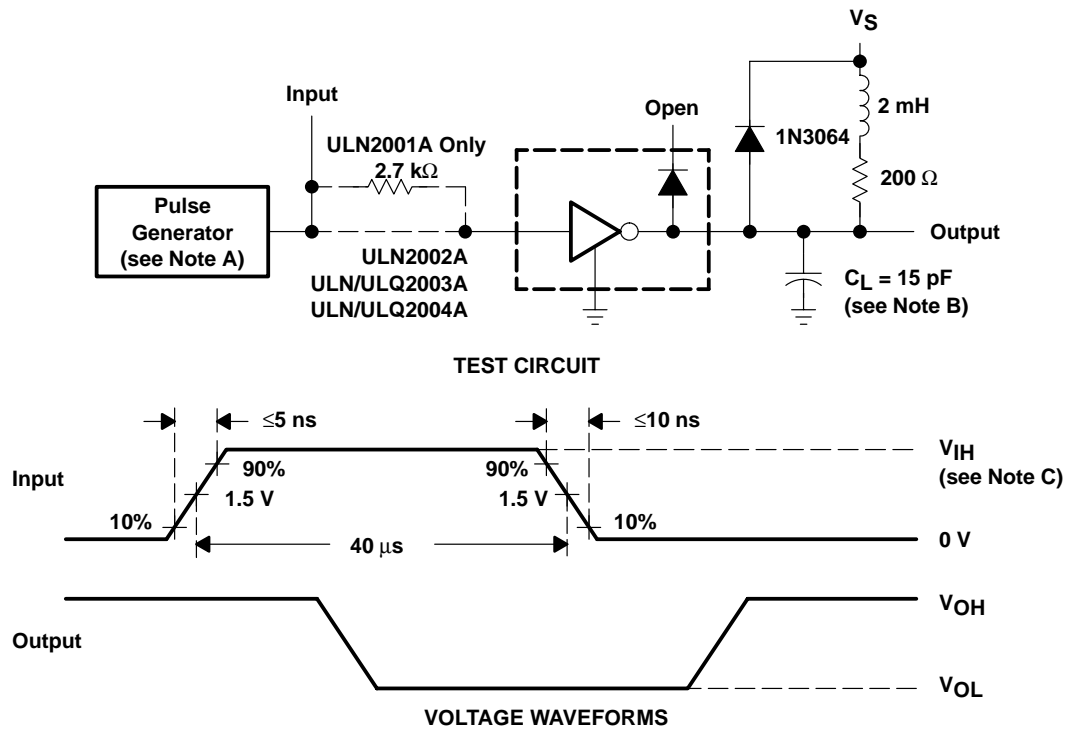


Figure 9. Propagation Delay-Time Waveforms



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. For testing the ULN2001A, the ULN2003A, and the ULQ2003A, $V_{IH} = 3 \text{ V}$; for the ULN2002A, $V_{IH} = 13 \text{ V}$; for the ULN2004A and the ULQ2004A, $V_{IH} = 8 \text{ V}$.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

**COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(ONE DARLINGTON)**

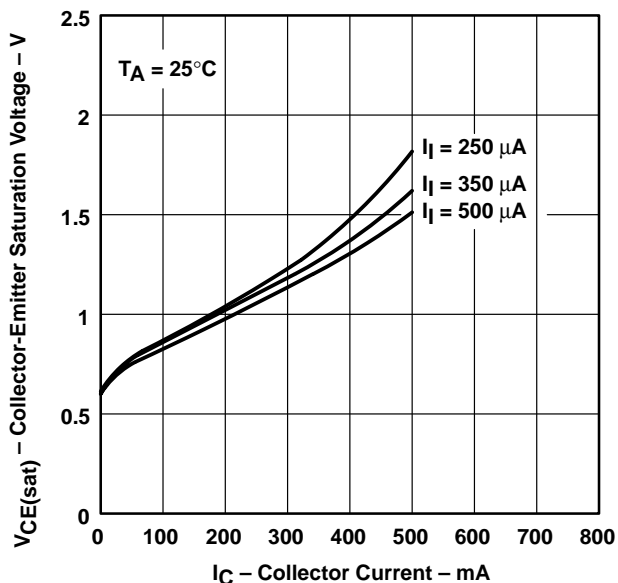


Figure 11

**COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
TOTAL COLLECTOR CURRENT
(TWO DARLINGTONS IN PARALLEL)**

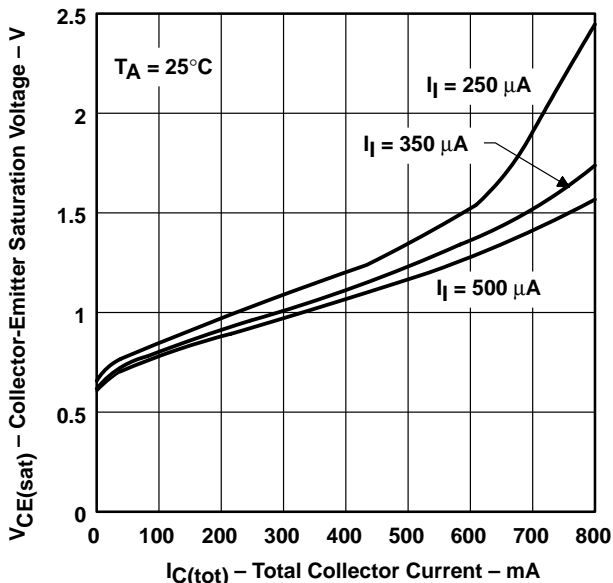


Figure 12

**COLLECTOR CURRENT
vs
INPUT CURRENT**

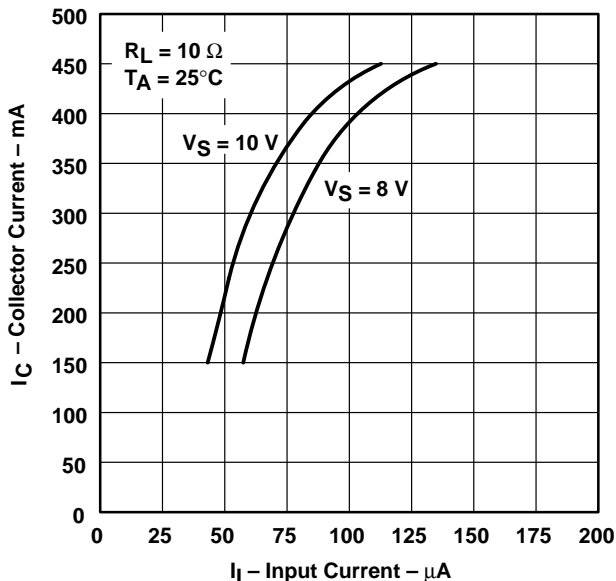


Figure 13



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THERMAL INFORMATION

D PACKAGE
 MAXIMUM COLLECTOR CURRENT
 vs
 DUTY CYCLE

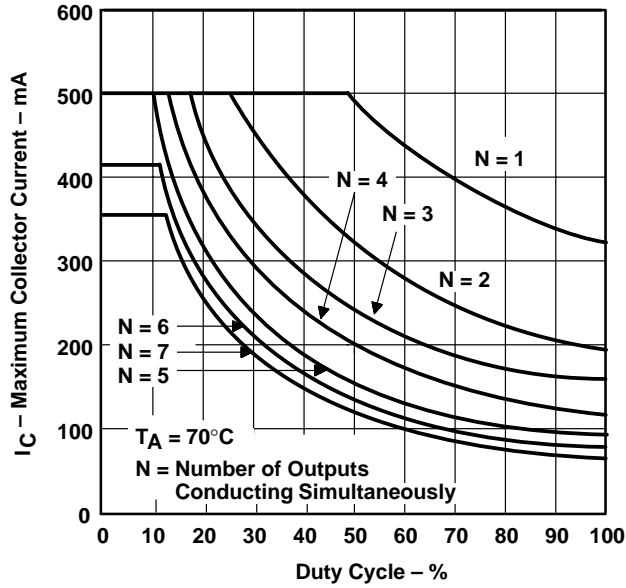


Figure 14

N PACKAGE
 MAXIMUM COLLECTOR CURRENT
 vs
 DUTY CYCLE

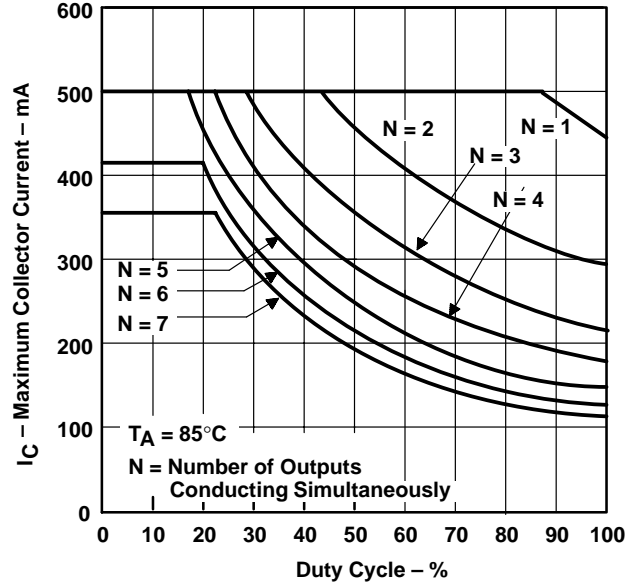


Figure 15

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APPLICATION INFORMATION

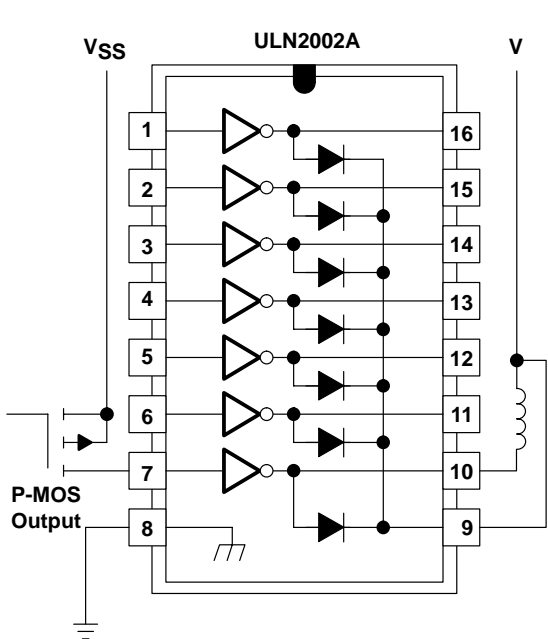


Figure 16. P-MOS to Load

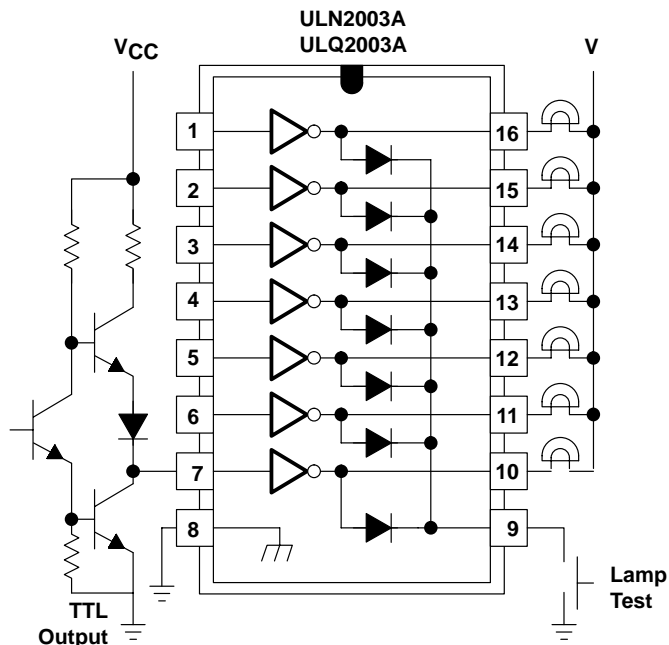


Figure 17. TTL to Load

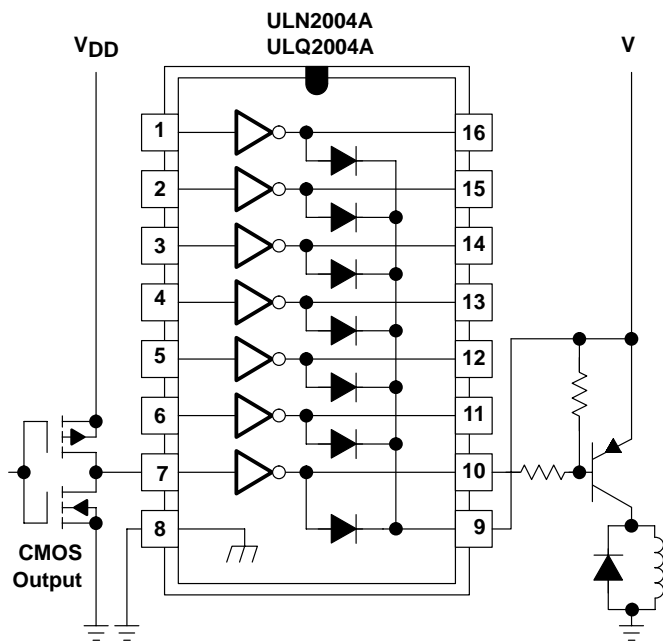


Figure 18. Buffer for Higher Current Loads

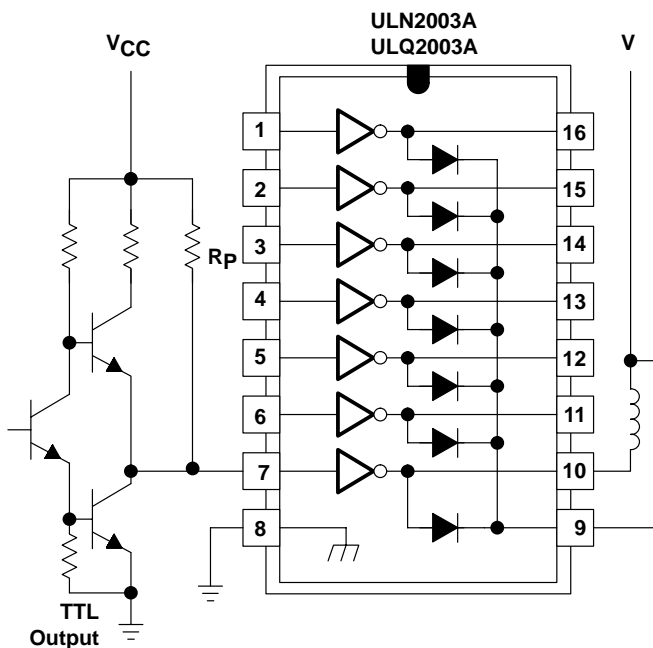


Figure 19. Use of Pullup Resistors
to Increase Drive Current

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