November 1994

National Semiconductor

LMC6022
Low Power CMOS Dual Operational Amplifier

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V⁻, low input bias current, and voltage gain (into 100k and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

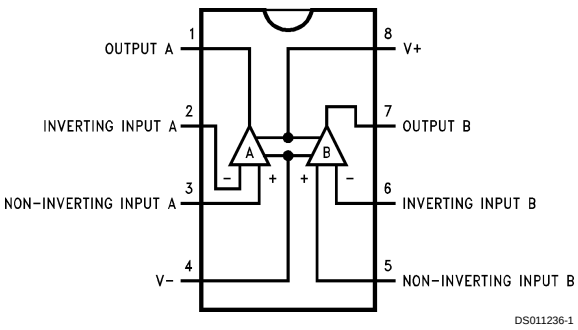
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain: 120 dB
- Low offset voltage drift: 2.5 µV/°C
- Ultra low input bias current: 40 fA
- Input common-mode range includes V⁻
- Operating range from +5V to +15V supply
- Low distortion: 0.01% at 1 kHz
- Slew rate: 0.11 V/µs
- Micropower operation: 0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

8-Pin DIP/SO



Top View

Ordering Information

Temperature Range Industrial $-40^{\circ}C \le T_J \le +85^{\circ}C$	Package	NSC Drawing	Transport Media
LMC6022IN	8-Pin Molded DIP	N08E	Rail
LMC6022IM	8-Pin Small Outline	M08A	Rail Tape and Reel

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Absolute Maximum Ratings (Note 1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature	150˚C
ESD Tolerance (Note 4)	1000V
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Current at Input Pin	±5 mA
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 12)

Operating Ratings

Temperature Range	$-40˚C \le T_J \le +85˚C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101˚C/W
8-Pin SO	165˚C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25˚C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9	mV
				11	max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		µV/˚C
I_B	Input Bias Current		0.04		pA
				200	max
I_{OS}	Input Offset Current		0.01		pA
				100	max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$, $V^+ = 15V$	83	63	dB
				61	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63	dB
				61	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74	dB
				73	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V, For CMRR ≥ 50 dB	−0.4	−0.1	V
				0	max
			$V^+ - 1.9$	$V^+ - 2.3$	V
				$V^+ - 2.5$	min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7) Sourcing	1000	200	V/mV
				100	min
		Sinking	500	90	V/mV
				40	min
		$R_L = 5 k\Omega$ (Note 7) Sourcing	1000	100	V/mV
				75	min
		Sinking	250	50	V/mV
				20	min

DC Electrical Characteristics (Continued)

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_O	Output Voltage Swing	V^+ = 5V	4.987	4.40	V
		R_L = 100 kΩ to 2.5V		**4.43**	min
			0.004	0.06	V
				0.09	max
		V^+ = 5V	4.940	4.20	V
		R_L = 5 kΩ to 2.5V		**4.00**	min
			0.040	0.25	V
				0.35	max
		V^+ = 15V	14.970	14.00	V
		R_L = 100 kΩ to 7.5V		**13.90**	min
			0.007	0.06	V
				0.09	max
		V^+ = 15V	14.840	13.70	V
		R_L = 5 kΩ to 7.5V		**13.50**	min
			0.110	0.32	V
				0.40	max
I_O	Output Current	V^+ = 5V	22	13	mA
		Sourcing, V_O = 0V		**9**	min
		Sinking, V_O = 5V	21	13	mA
		(Note 2)		**9**	min
		V^+ = 15V	40	23	mA
		Sourcing, V_O = 0V		**15**	min
		Sinking, V_O = 13V	39	23	mA
		(Note 12)		**15**	min
I_S	Supply Current	Both Amplifiers	86	140	µA
		V_O = 1.5V		**165**	max

AC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless other otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/µs min
GBW	Gain-Bandwidth Product		0.35		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

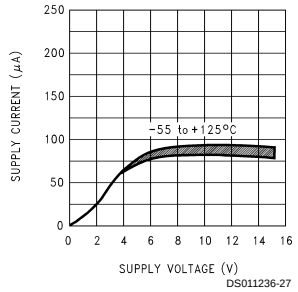
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified

Supply Current vs Supply Voltage



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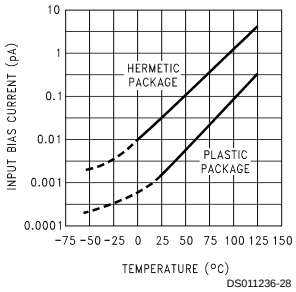
Input Bias Current vs Temperature



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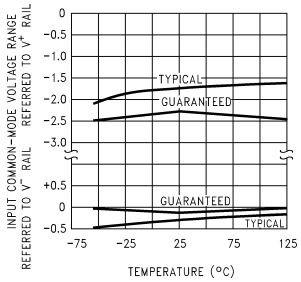
Input Common-Mode Voltage Range vs Temperature



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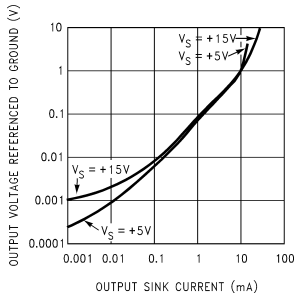
Output Characteristics Current Sinking



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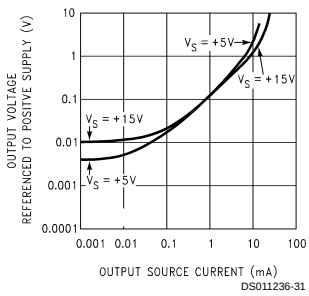
Output Characteristics Current Sourcing



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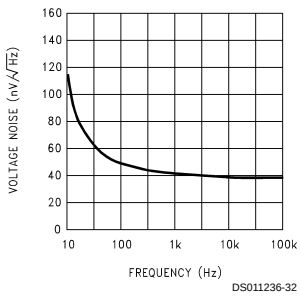
Input Voltage Noise vs Frequency



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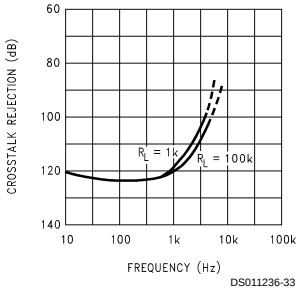
Crosstalk Rejection vs Frequency



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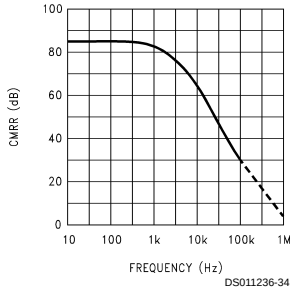
CMRR vs Frequency



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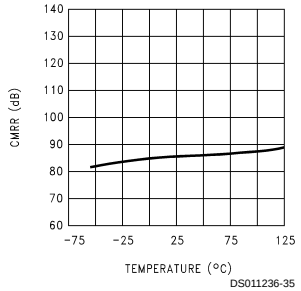
CMRR vs Temperature



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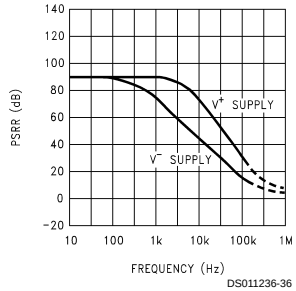
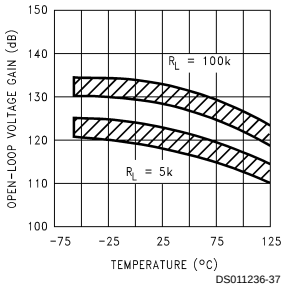
Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

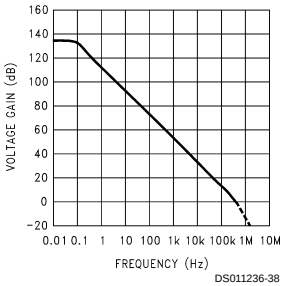
Power Supply Rejection Ratio vs Frequency



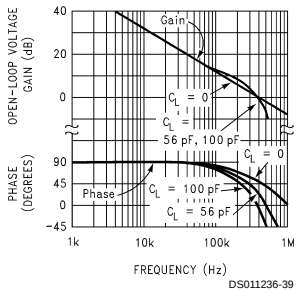
Open-Loop Voltage Gain vs Temperature



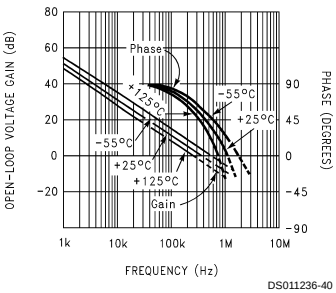
Open-Loop Frequency Response



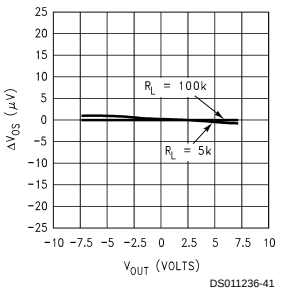
Gain and Phase Responses vs Load Capacitance



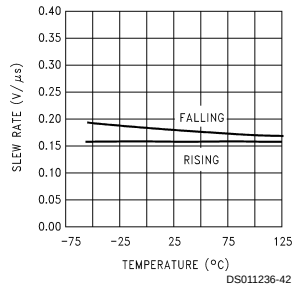
Gain and Phase Responses vs Temperature



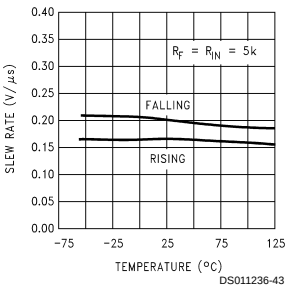
Gain Error (V_{OS} vs V_{OUT})



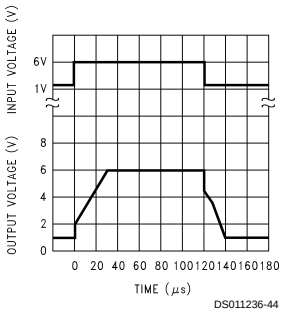
Non-Inverting Slew Rate vs Temperature



Inverting Slew Rate vs Temperature

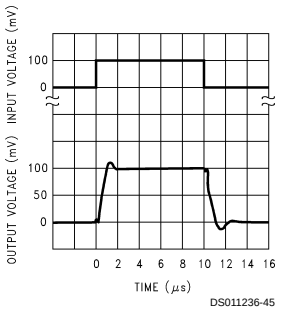


Large-Signal Pulse Non-Inverting Response (A_V = +1)



Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

Non-Inverting Small Signal Pulse Response (A_V = +1)



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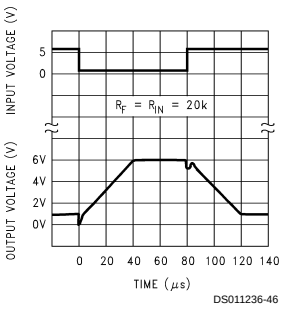
Inverting Large-Signal Pulse Response



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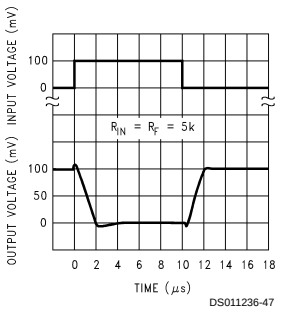
Inverting Small-Signal Pulse Response



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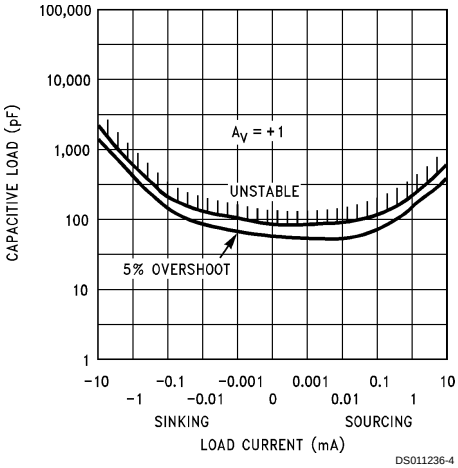
Stability vs Capacitive Load



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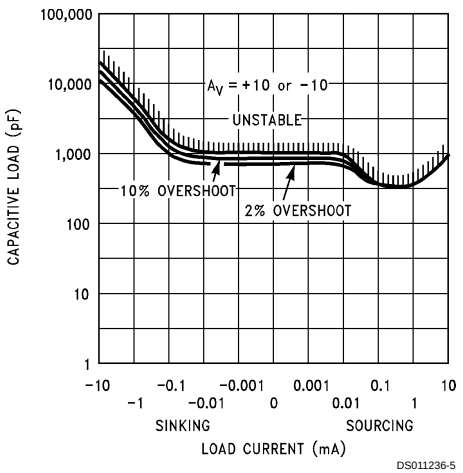
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Stability vs Capacitive Load



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Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

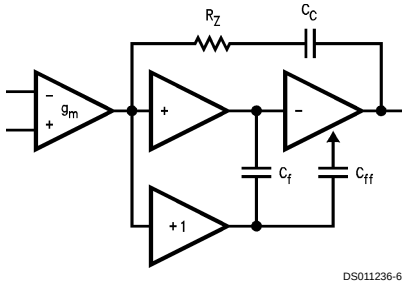

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FIGURE 1. LMC6022 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driv-

Application Hints (Continued)

ing load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

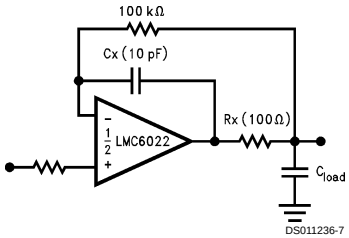


FIGURE 2. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3*). Typically a pull up resistor conducting 50 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

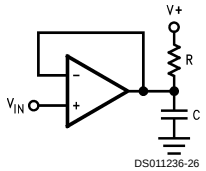


FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 5a*, *Figure 5b*, *Figure 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d*.

Application Hints (Continued)

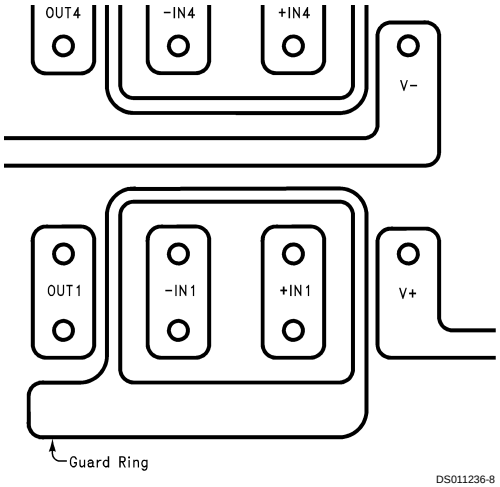
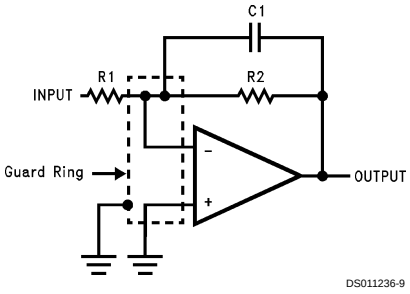
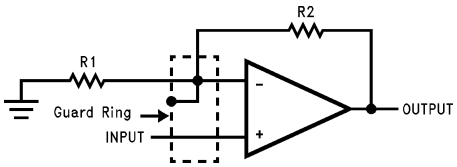


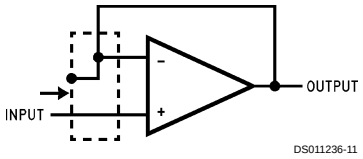
FIGURE 4. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)



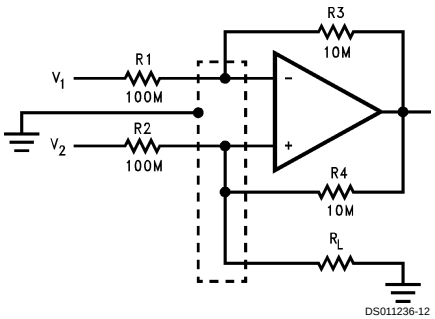
(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower

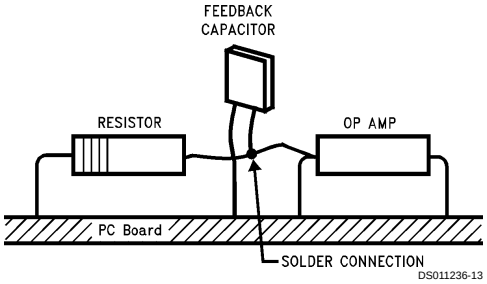


(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.

Application Hints (Continued)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

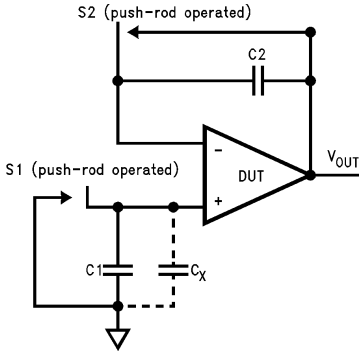


FIGURE 7. Simple Input Bias Current Test Circuit

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

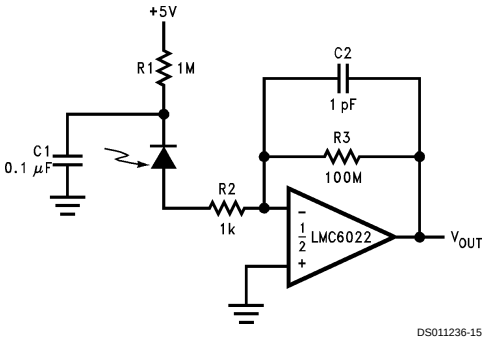
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

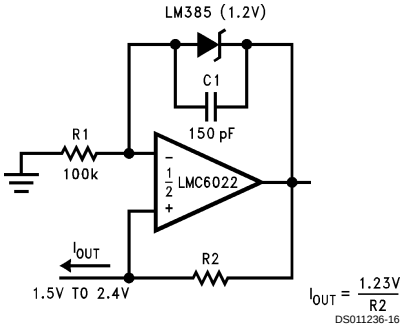
Typical Single-Supply Applications ($V+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter



Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

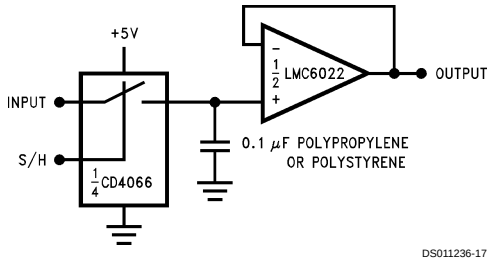
Micropower Current Source



(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

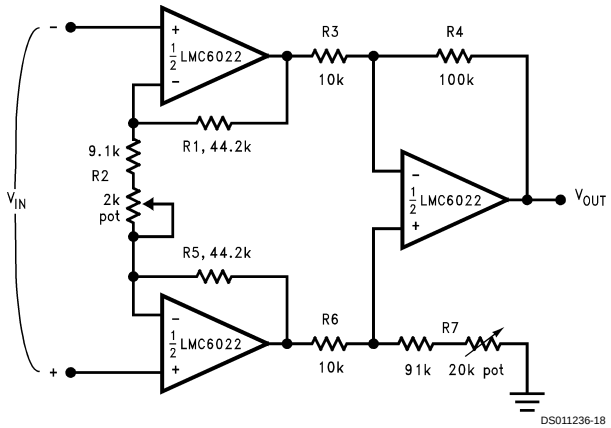
Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

Low-Leakage Sample-and-Hold



DS011236-17

Instrumentation Amplifier



DS011236-18

If R1 = R5, R3 = R6, and R4 = R7;
Then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

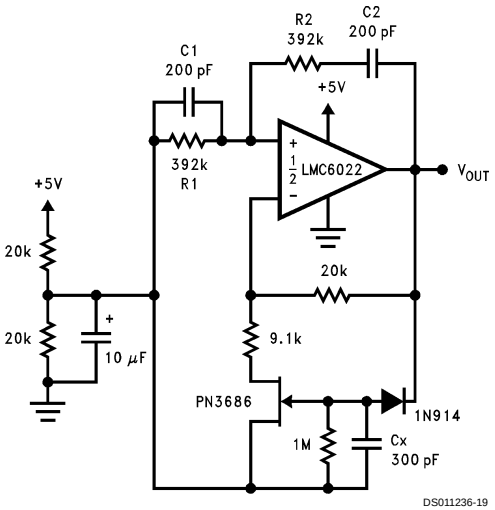
$\therefore A_V \approx 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications

($V+ = 5.0\ V_{DC}$) (Continued)

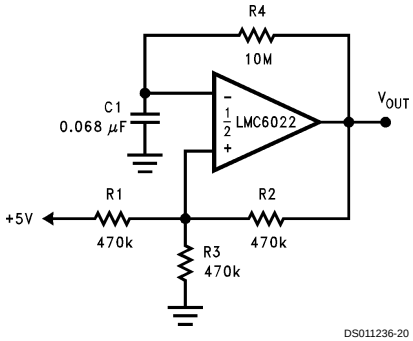
Sine-Wave Oscillator



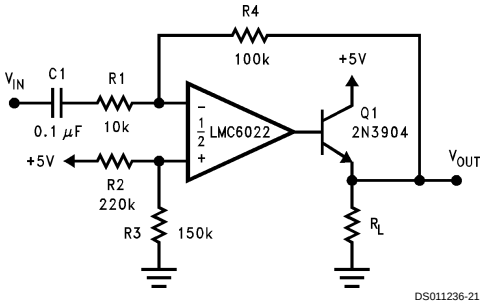
Oscillator frequency is determined by R1, R2, C1, and C2:
$f_{OSC} = 1/2\pi RC$
where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator

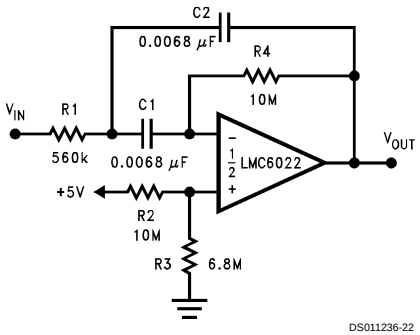


Power Amplifier



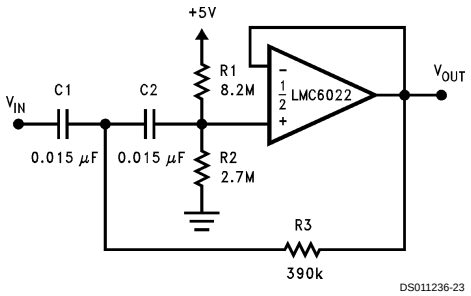
Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

10 Hz Bandpass Filter



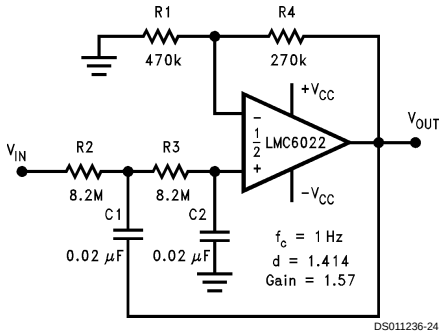
f_O = 10 Hz
Q = 2.1
Gain = −8.8

10 Hz High-Pass Filter (2 dB Dip)

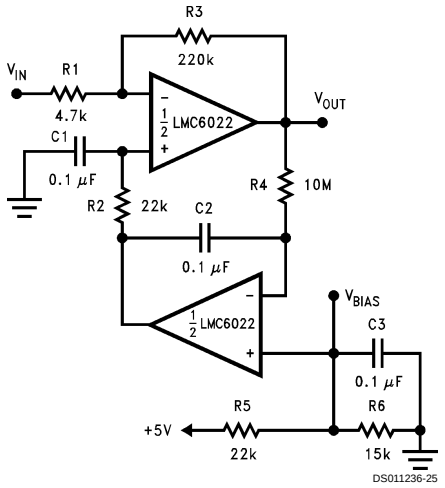


f_c = 10 Hz
d = 0.895
Gain = 1

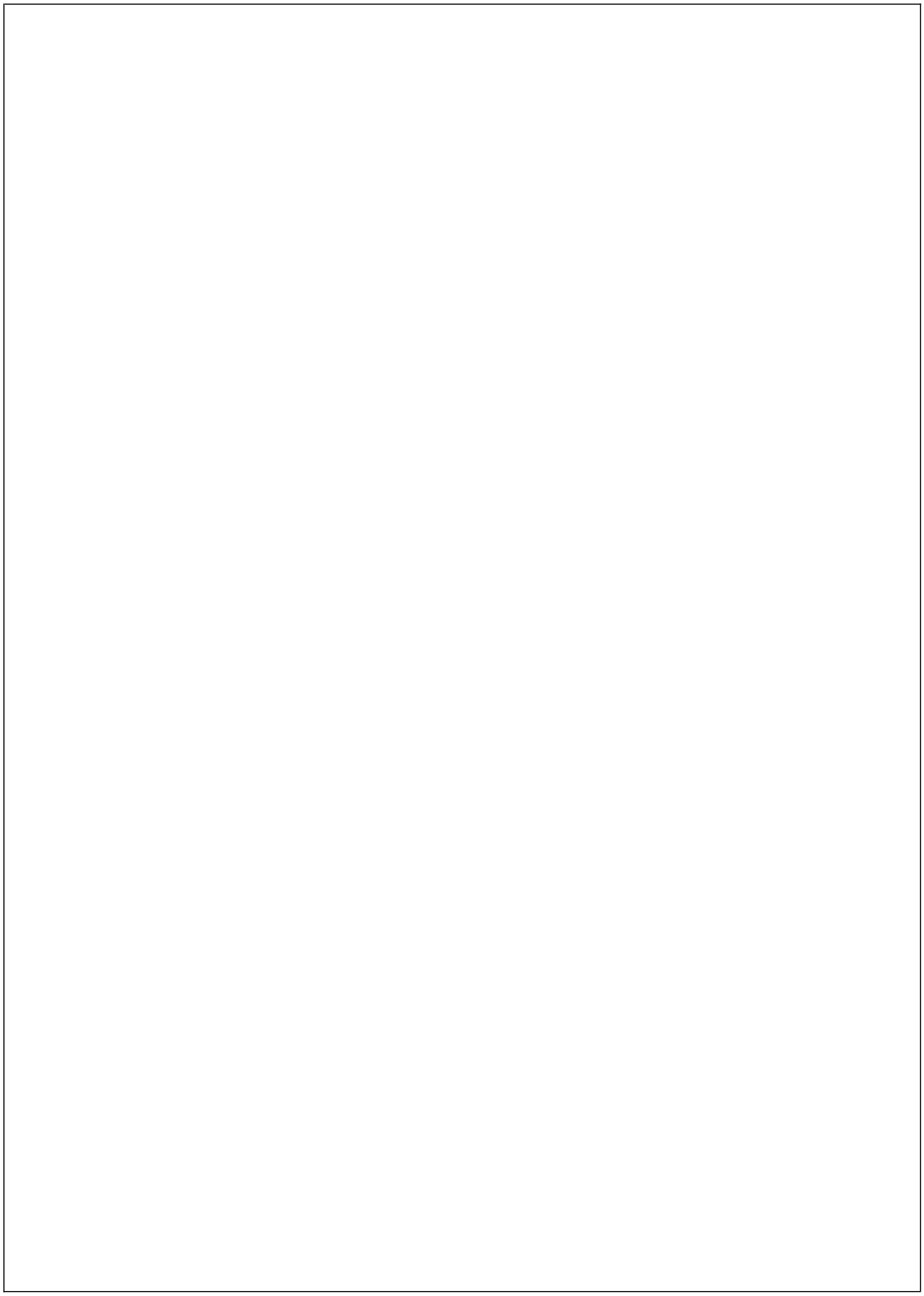
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



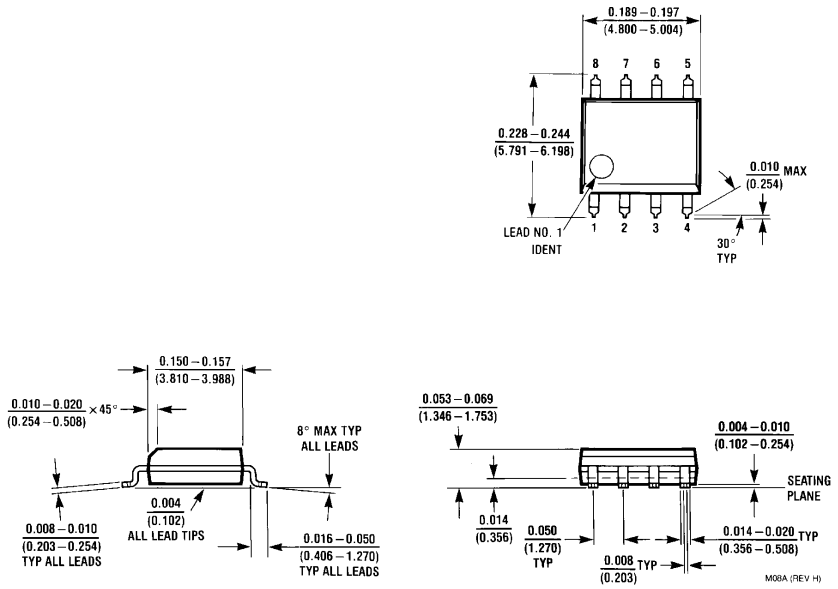
High Gain Amplifier with Offset Voltage Reduction



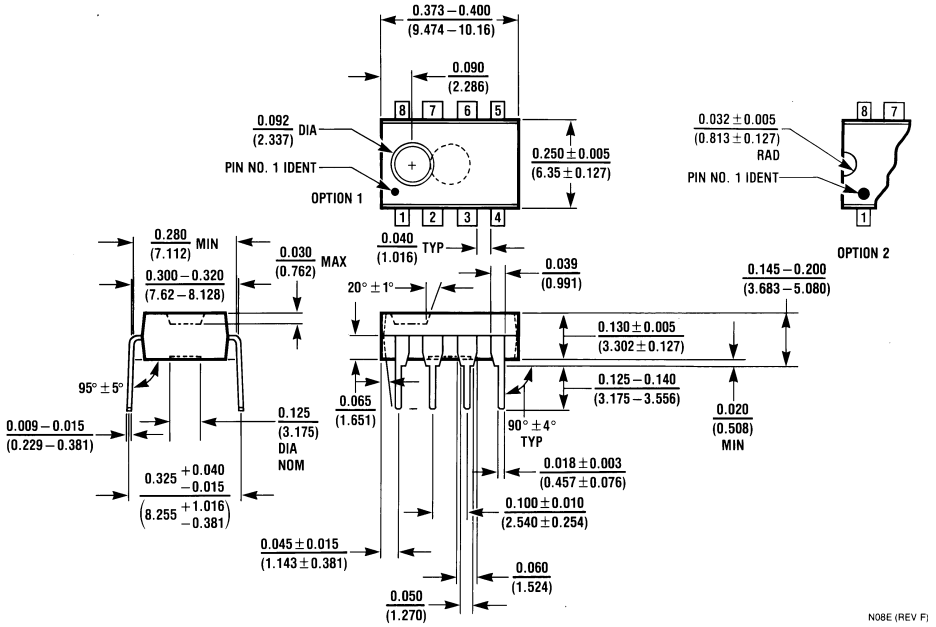
Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.



Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Small Outline Molded Package (M)
Order Number LMC6022IM
NS Package Number M08A



8-Pin Molded Dual-In-Line Package (N)
Order Number LMC6022IN
NS Package Number N08E

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