STMPE821

8-bit Xpander Logic™ with touchkey controller

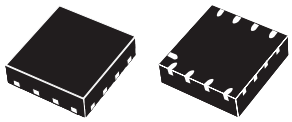
Preliminary Data

Features

- Up to 8 GPIOs
- Up to 8 touchkey capacitive touch inputs
- Operating voltage 1.8 - 5.5 V
- Internal regulator
- Interrupt output pin
- I^2C interface
- 8 kV HBM ESD protection
- 40 fF resolution, 128 steps capacitance measurement (5.0 pF dynamic range)
- Advanced data filtering (AFS)
- Environment tracking calibration (ETC)
- Individually adjustable touch variance (TVR) setting for all channels
- Adjustable environmental variance (EVR) for optimal calibration

Applications

- Mobile and smart phones
- Portable media players
- Game consoles



QFN16L
(2.6 x 1.8 mm)

Description

The STMPE821 is a GPIO (general purpose input/output) port expander able to interface a main digital ASIC via the two-line bidirectional bus (I^2C).

A separate GPIO expander is often used in mobile multimedia platforms to solve the problems of the limited amount of GPIOs typically available on the digital engine.

The STMPE821 offers great flexibility, as each I/O can be configured as input, output or specific functions. The device has been designed with very low quiescent current and includes a wakeup feature for each I/O, to optimize the power consumption of the device.

Table 1. Device summary

Order code	Package	Packing
STMPE821QTR	QFN16L (2.6 x 1.8 mm)	Tape and reel

Contents

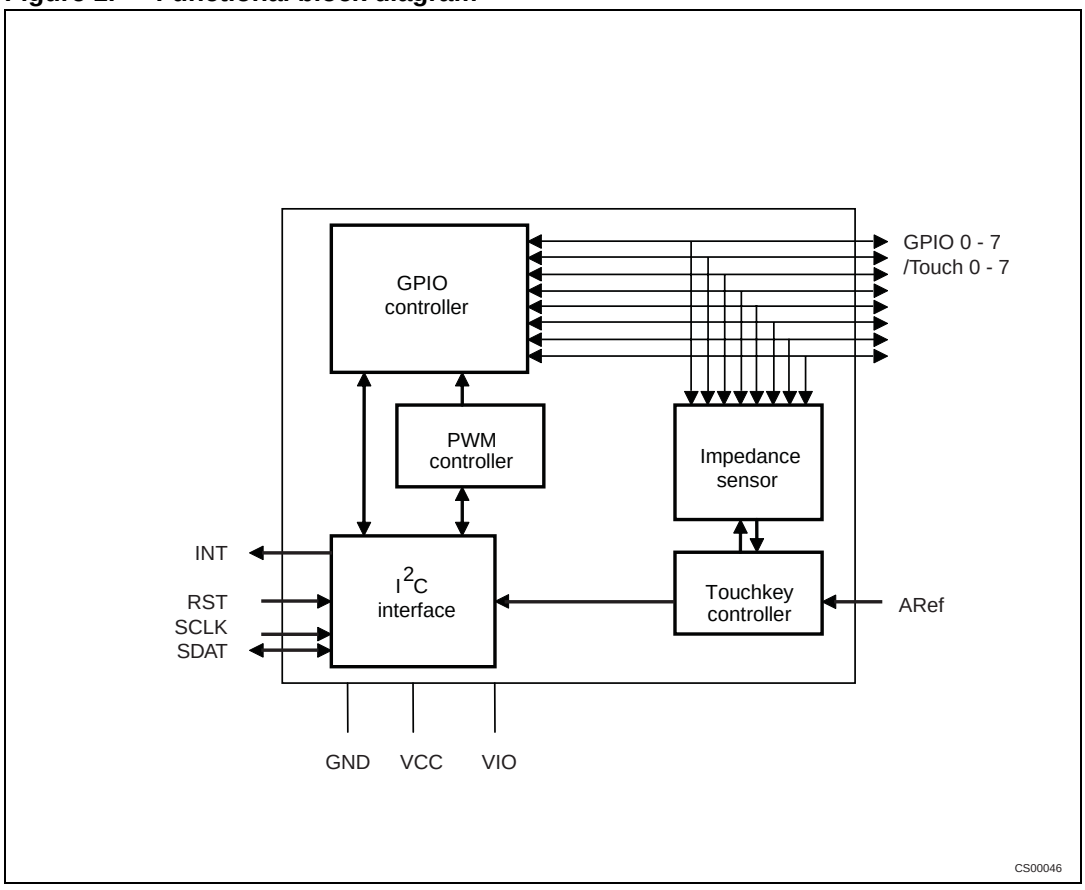
1 STMPE821 functional overview

The STMPE821 consists of the following blocks:

- GPIO controller
- PWM controller
- Impedance sensor
- Touchkey controller
- I^2C interface

1.1 STMPE821 block diagram

Figure 1. Functional block diagram



1.2 Pin assignment and function

Figure 2. STMPE821 pin assignment (top view)

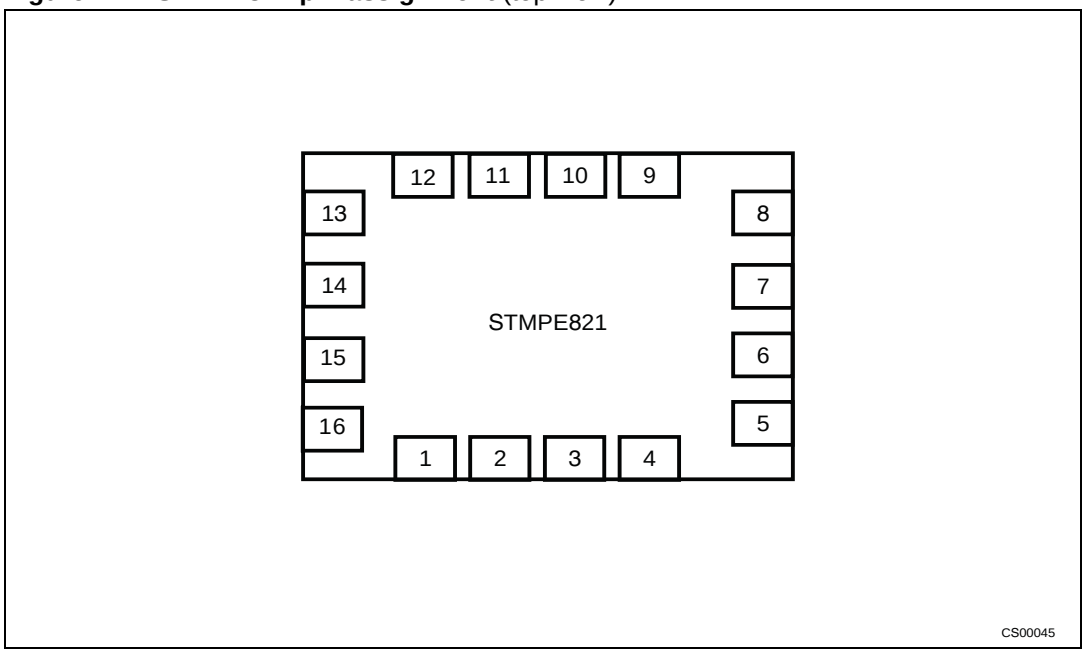


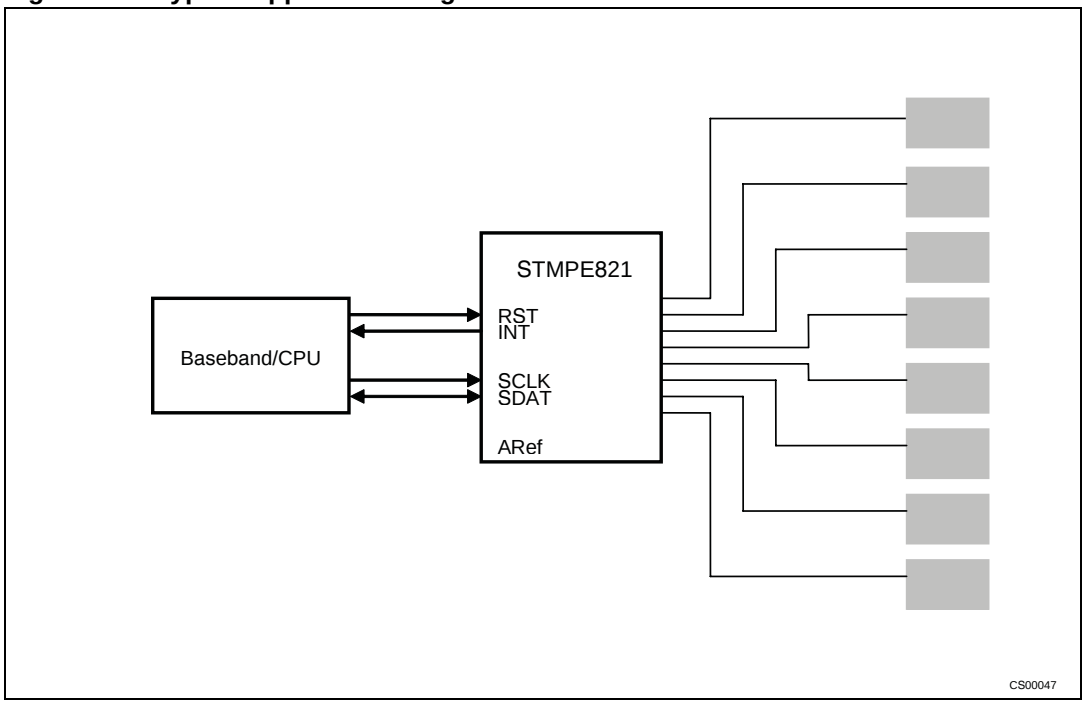
Table 2. Pin assignments and function

Pin number	Pin name	Description
1	GPIO_2/Touch_2	GPIO 2
2	GPIO_1/Touch_1	GPIO 1
3	GPIO_0/Touch_0	GPIO 0
4	ARef	Reference capacitor for touch sensor
5	RST	RESET (active low)
6	SDA	I^2C data
7	SCL	I^2C clock
8	INT	INT output
9	GND	GND
10	V_{CC}	Supply voltage for I^2C block
11	V_{IO}	Supply voltage for GPIO and internal regulator
12	GPIO_7/Touch_7	GPIO 7
13	GPIO_6/Touch_6	GPIO 6
14	GPIO_5/Touch_5	GPIO 5
15	GPIO_4/Touch_4	GPIO 4
16	GPIO_3/Touch_3	GPIO 3

1.3 STMPE821 typical application

The STMPE821 is able to support up to 8 channel capacitive sensors.

Figure 3. Typical application diagram

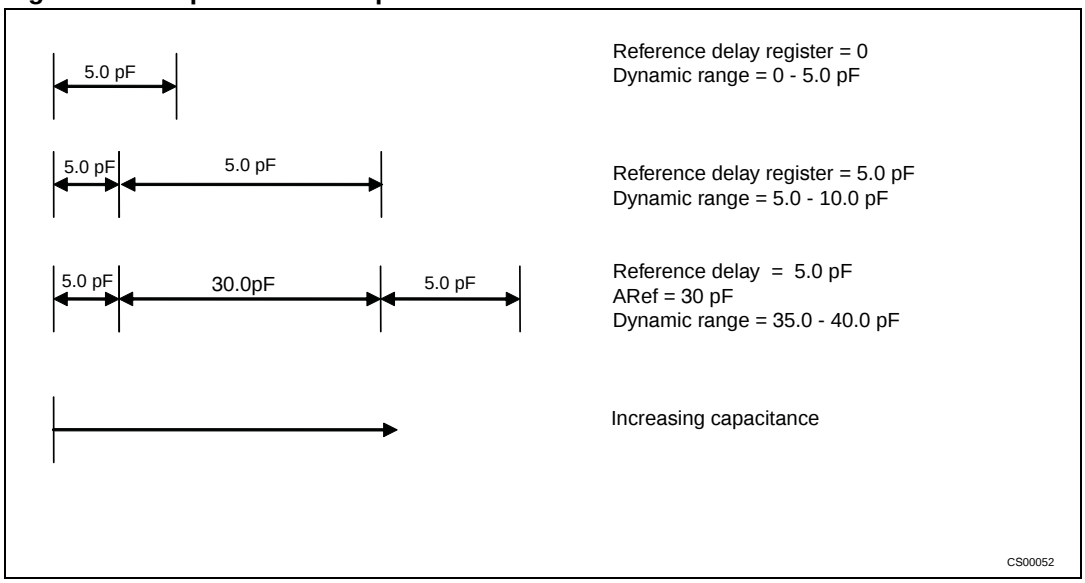


2 Capacitive compensation

The STMPE821 is capable to measuring up to 5.0 pF in capacitance difference between the reference point (Zref) and the individual channels. In the case where the PCB connection between the sensor pads and the device is too long, the "REFERENCE DELAY" register is able to shift the reference by up to 5.0 pF, allowing the TOUCH channels to measure added capacitance 5.0 pF with offset of 5.0 pF, as shown in following diagram.

In case this is still not enough to compensate for the capacitance on sensor lines (due to very long sensor trace), an external capacitor of up to 30 pF can be connected at the A_Ref pin. This allows to further shift up the dynamic range of the capacitance measurement.

Figure 4. Capacitance compensation



The sensed capacitance is accessible to host through the "IMPEDANCE" registers.

2.1 Calibration algorithm

The STMPE821 maintains 2 parameters for each TOUCH channel: TVR and CALIBRATED IMPEDANCE. CALIBRATED IMPEDANCE is an internal reference of which, if the currently measured IMPEDANCE exceeds the CALIBRATED IMPEDANCE by a magnitude of TVR, it is considered a TOUCH.

If the IMPEDANCE is more than the CALIBRATED IMPEDANCE, but the magnitude does not exceed CALIBRATED IMPEDANCE by TVR, it is not considered a TOUCH. In this case, 2 scenarios are possible:

1. Environmental changes has caused the IMPEDANCE to increase

2. Finger is near the sensing pad, but not near enough

In case 1, the change in IMPEDANCE is expected to be small, as environmental changes are normally gradual. A value "EVR" is maintained to specify the maximum IMPEDANCE change that is still considered an environmental change.

Table 3. Calibration action under different scenarios

Scenario	Touch sensing and calibration action
IMP>CALIBRATED IMP + TVR	Touch sensing and calibration action
	No touch, no calibration
IMP<CALIBRATED IMP + TVR IMP>CALIBRATED IMP + EVR	No touch, no calibration
IMP<CALIBRATED IMP + TVR IMP<CALIBRATED IMP + EVR	No touch, new CALIBRATED IMP = previous
IMP>CALIBRATED IMP	CALIBRATED IMP + change in IMP
IMP<CALIBRATED IMP	No touch, new CALIBRATED IMP = new IMP

ETC WAIT register state a period of time of which, all TOUCH inputs must remain "NO TOUCH" for the next calibration to be carried out.

CAL INTERVAL states the period of time between successive calibrations when there are prolonged NO TOUCH condition.

2.1.1 Noise filtering

When the STMPE821 is operating in the vicinity of highly emissive circuits (DC-DC converter, PWM controller/drive etc), the sensor inputs will be affected by high-frequency noise. In this situation, the time-integrating function could be used to distinguish between real touch, or emission-related false touch.

The INTEGRATION TIME and STRENGTH THRES registers are used to configure the time-integrating function of STMPE821.

2.1.2 Data filtering

The output from the calibration unit is an instantaneous "TOUCH" or "NO TOUCH" status. This output is directed to the filtering stage where the TOUCH is integrated across a programmable period of time. The output of the integration stage would be a "STRENGTH" (in STRENGTH register) that indicates the number of times a "TOUCH" is seen, across the integration period.

The "STRENGTH" is then compared with the value in "STRENGTH THRESHOLD" register. If STRENGTH exceeds the STRENGTH THRESHOLD, this is considered a final, filtered TOUCH status.

In data filtering stage, 3 modes of operation is supported:

Mode 1: Only the “touch” channel with highest STRENGTH is taken

Mode 2: All the “touch” channels with STRENGTH > STRENGTH THRESHOLD is taken

Mode 3: The 2 “touch” channel with the highest STRENGTH is taken

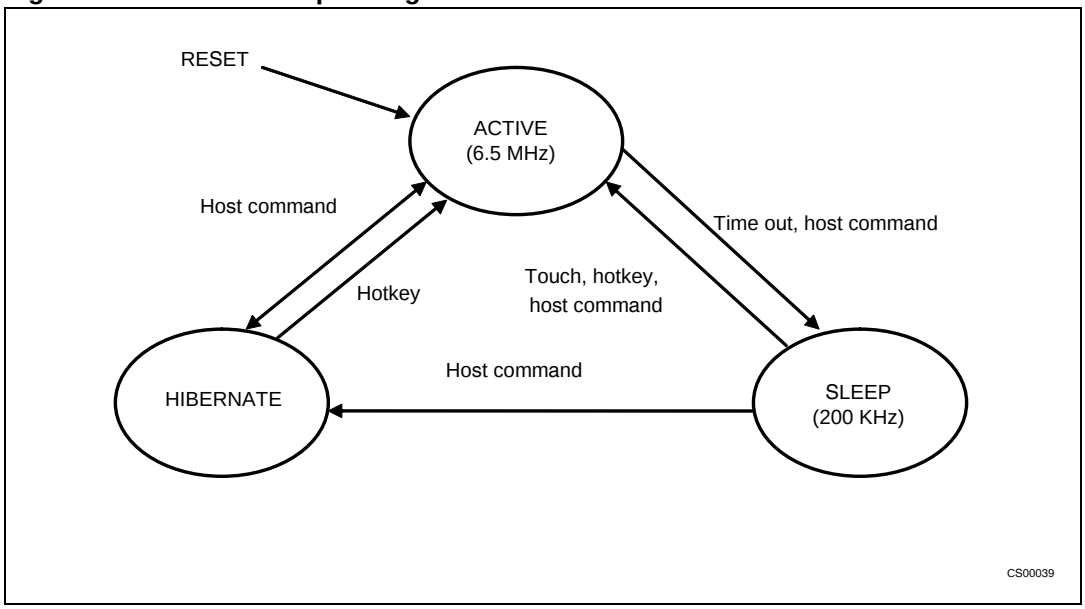
These modes are selected using the FEATURE SELECTOR register.

The final, filtered data is accessible through the Touch Byte register.

2.2 Power management

The STMPE821 operates in 3 states.

Figure 5. STMPE821 operating states



On RESET, the STMPE821 enters the ACTIVE state immediately.

Upon a fixed period of inactivity, the device enters into the SLEEP state. Any touch activity in SLEEP state would cause the device to go back to ACTIVE state.

In SLEEP mode:

-Calibration continues if F2A bit is set in CONTROL register

-Calibration stops if F2A bit is NOT set in CONTROL register (IDLE mode)

If no touch activity is expected, the host may set the device into HIBERNATE state to save power.

3 Power schemes

The STMPE821 can be powered by a 1.8 V supply directly, or 3.0 - 3.6 V supply through the internal voltage regulator. V_{IO} powers all the GPIOs directly, if LED driving is required on the GPIO, V_{IO} should be at least 3.3 V.

Figure 6. Power using the internal regulator

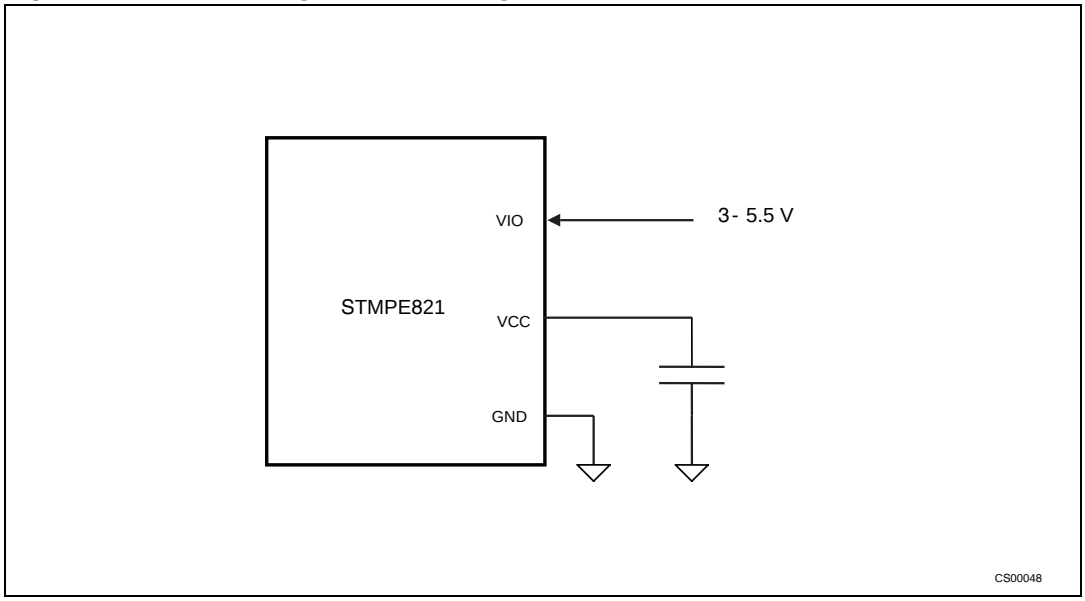
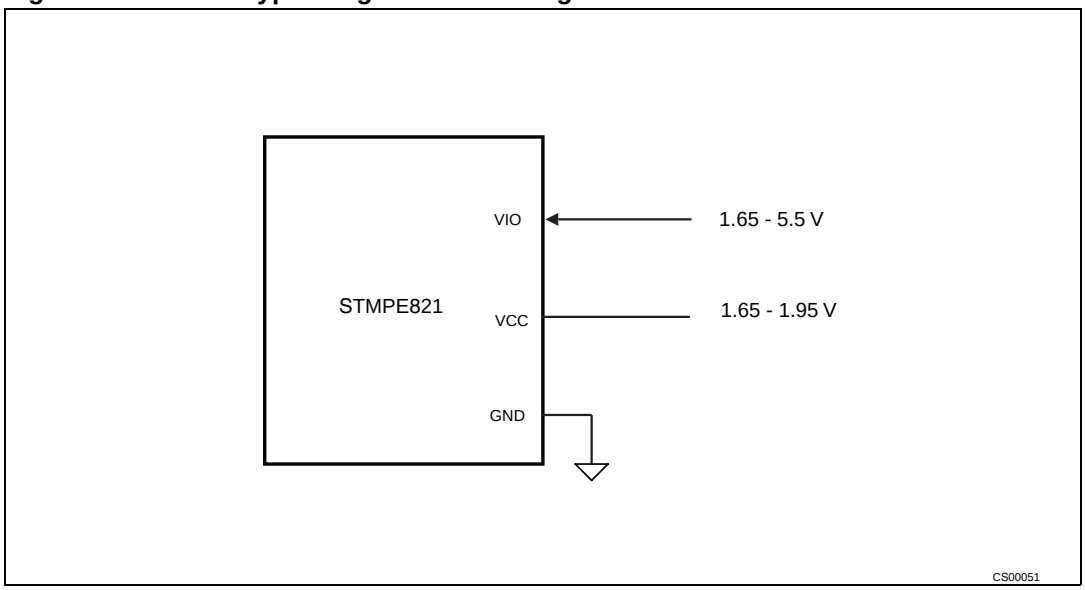


Figure 7. Power bypassing the internal regulator



4 I²C interface

The features that are supported by the I²C interface are the following ones:

- I²C slave device
- Compliant to Philips I²C specification version 2.1
- Supports standard (up to 100 kbps) and fast (up to 400 kbps) modes.
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- I²C address is 0x58 (0xB0/0xB1 for write/read, including the LSB)

Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I²C transaction. A Stop condition at the end of a write command stops the write operation to registers.

Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls the SDATA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in high state if it would to not acknowledge the receipt of the data.

Data Input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

Memory addressing

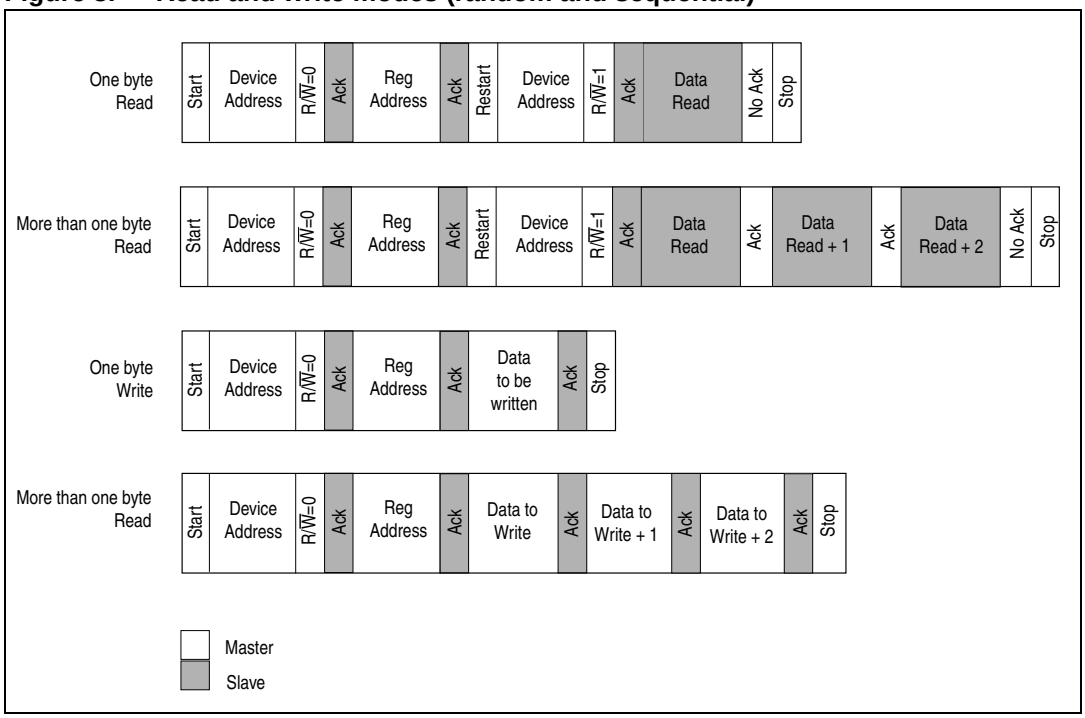
For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/$\overline{\text{WRITE}}$ bit (R/$\overline{\text{W}}$). The bit is set to 1 for read and 0 for write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

Table 4. Operation modes

Mode	Byte	Programming sequence
Read	≥1	Start, Device address, R/$\overline{W}$ = 0, Register address to be read
		Restart, Device address, R/$\overline{W}$ = 1, Data Read, STOP
		If no Stop is issued, the Data Read can be continuously performed. If the register address falls within the range that allows an address auto-increment, then the register address auto-increments internally after every byte of data being read. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment. An example of such a non-increment address is FIFO
Write	≥1	Start, Device address, R/$\overline{W}$ = 0, Register address to be written, Data Write, Stop
		If no Stop is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then the register address auto-increments internally after every byte of data being written in. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment. An example of a non-increment address is Data port for initializing the PWM commands.

Figure 8. Read and write modes (random and sequential)



5 Register map and function description

This section lists and describes the registers of the STMPE821 device, starting with a register map and then provides detailed descriptions of register types.

Table 5. Register summary map table

Address	Register name	Bit	Type	Reset value	Function
0x00	CHIP_ID_0	8	R	0x08	Device identification
0x01	CHIP_ID_1	8	R	0x21	Device identification
0x02	ID_VER	8	R	0x01	Revision number
0x03	SYS_CFG_1	8	R/W	0x00	System configuration 1
0x04	SYS_CFG_2	8	R/W	0xEF	System configuration 2
0x08	INT_CTRL	8	R/W	0x01	Interrupt control register
0x09	INT_EN	8	R/W	0x01	Interrupt enable register
0x0A	INT_STA	8	R	0x01	Interrupt status register
0x0B	GPIO__INT_EN_lsb	8	R/W	0x00	GPIO interrupt enable register
0x0C	GPIO__INT_EN_msb	8	R/W	0x00	GPIO interrupt enable register
0x0D	GPIO_INT_STA_lsb	8	R/W	0x00	GPIO interrupt status register
0x0E	GPIO_INT_STA_msb	8	R/W	0x00	GPIO interrupt status register
0x10	GPIO_MR	8	R/W	0x00	GPIO monitor pin
0x12	GPIO_SET	8	R/W	0x00	GPIO set pin state register
0x14	GPIO_DIR	8	R/W	0x00	GPIO set pin direction register
0x16	GPIO_FUNCT	8	R/W	0x00	GPIO function register
0x18	TOUCH_FIFO	64	R	0x00	Fifo access for touch data buffer
0x20	FEATURE_SEL	8	R/W	0x04	Feature selection
0x21	ETC_WAIT	8	R/W	0x27	Wait time
0x22	CAL_INTERVAL	8	R/W	0x30	Calibration interval
0x23	INTEGRATION_ TIME	8	R/W	0x0F	Integration time
0x25	CTRL	8	R/W	0x00	Control
0x26	INT_MASK	8	R/W	0x08	Interrupt mask
0x27	INT_CLR	8	R/W	0x00	Interrupt clear
0x28	FILTER_PERIOD	8	R/W	0x00	Filter period
0x29	FILTER_THRESHOL D	8	R/W	0x00	Filter threshold
0x2A	REF_DLY	8	R/W	0x00	Reference delay
0x30 - 0x37	TVR	8	R/W	0x08	Touch variance setting

Table 5. Register summary map table (continued)

Address	Register name	Bit	Type	Reset value	Function
0x40	EVR	8	R/W	0x04	Enviromental variance
0x50 - 0x57	STRENGTH_THRES [0-7]	8	R/W	0x01	Setting of strength threshold for each channel
0x60 - 0x67	STRENGTH [0-7]	8	R	0x00	Strenght
0x70 - 0x77	CAL_IMPEDANCE [0-7]	8	R	0x00	Calibrated impedance
0x80 - 0x87	IMPEDANCE [0-7]	8	R	0x00	Impedance
0x90	TOUCH_BYTE_L	8	R	0x00	Touch sensing data output
0x91	TOUCH_BYTE_H	8	R	0x00	Touch sensing data output
0x92	INT_PENDING	8	R/W	0x00	Status of GINT interrupt sources
0xA0	PWM_OFF_OUTPUT	8	R/W	0x00	PWM group control
0xA1	MASTER_EN	8	R/W	0x00	Master enable
0xB0	PWM0_SET	8	R/W	0x00	PWM 0 setup
0xB1	PWM0_CTRL	8	R/W	0x00	PWM 0 control
0xB2	PWM0_RAMP_RATE	8	R/W	0x00	PWM 0 ramp rate
0xB4	PWM1_SET	8	R/W	0x00	PWM 1 setup
0xB5	PWM1_CTRL	8	R/W	0x00	PWM 1 control
0xB6	PWM1_RAMP_RATE	8	R/W	0x00	PWM 1 ramp rate
0xB8	PWM2_SET	8	R/W	0x00	PWM 2 setup
0xB9	PWM2_CTRL	8	R/W	0x00	PWM 2 control
0xBA	PWM2_RAMP_RATE	8	R/W	0x00	PWM 2 ramp rate
0xBC	PWM3_SET	8	R/W	0x00	PWM 3 setup
0xBD	PWM3_CTRL	8	R/W	0x00	PWM 3 control
0xBE	PWM3_RAMP_RATE	8	R/W	0x00	PWM 3 ramp rate

6 System and identification registers

Table 6. System and identification registers map

Address	Register name	Bit	Type	Reset	Function
0x00	CHIP_ID_0	16	R	0x08	Device identification
0x01	CHIP_ID_1	16	R	0x21	Device identification
0x02	ID_VER	8	R	0x01	Revision number
0x03	SYS_CFG_1	8	R/W	0x00	System configuration 1
0x04	SYS_CFG_2	8	R/W	0xEF	System configuration 2

CHIP_ID_x Device identification

Address: 0x00, 0x01

Type: R

Reset: 0x08, 0x21

Description: 16-bit device identification

ID_VER Revision number

Address: 0x02

Type: R

Reset: 0x01

Description: 16-bit revision number

SYS_CFG_1 System configuration 1

7	6	5	4	3	2	1	0
RESERVED				SLEEP	WARM_RESET	SOFT_RESET	HIBERNATE

Address: 0x03

Type: R/W

Reset: 0x00

Description: The reset control register enables to reset the device

[7:4] RESERVED

[3] **SLEEP**:
Write ‘1’ to enable sleep mode

[2] **WARM_RESET**:
Write ‘1’ to initiate a warm reset. Register content remains, state machine reset.

[1] **SOFT_RESET**:
Write ‘1’ to initiate a soft reset. All registers content and state machines reset.

[0] **HIBERNATE**: Force the device into hibernation mode.
Write ‘1’ to enter the hibernate mode,

SYS_CFG_2 System configuration 2

7	6	5	4	3	2	1	0
SENSOR CLOCK 2	SENSOR CLOCK 1	SENSOR CLOCK 0	–	PWM CLOCK DISABLE	GPIO CLOCK DISABLE	FIFO CLOCK DISABLE	TOUCH CLOCK DISABLE

Address: 0x04

Type: R/W

Reset: 0xEF

Description: This register enables to switch off the clock supply

[7:5] **SENSOR CLOCK**: See description in the table below.

[4] **RESERVED**

[3] **PWM CLOCK DISABLE**:
Write ‘1’ to disable the clock to PWM unit.

[2] **GPIO CLOCK DISABLE**:
Write ‘1’ to disable the clock to GPIO unit. Note that GPIO clock is required for PWM operation.

[1] **FIFO CLOCK DISABLE**:
Write ‘1’ to disable the clock to FIFO unit. This must be set to ‘0’ if touch interrupt is required.

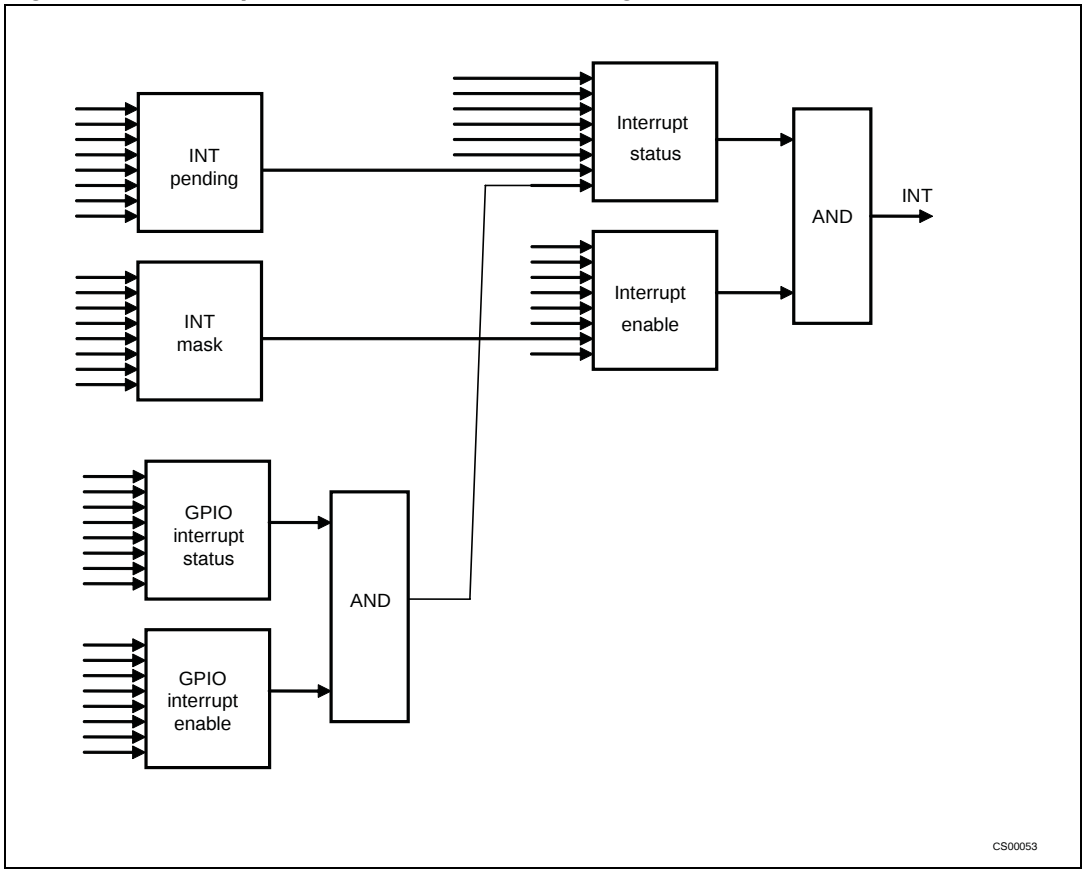
[0] **TOUCH CLOCK DISABLE**:
Write ‘1’ to disable the clock to TOUCH unit.

Table 7. Sensor clock setting

Mode	Divider	Sensor clock [2:0]	Active	Calibration	Idle
Operational (6.5 MHz)	1	000	12.8 KHz	100 KHz	400 Hz
	2	001	6.4 KHz	50 KHz	200 Hz
	4	010	3.2 KHz	25 KHz	100 Hz
	8	011	1.6 KHz	12.5 KHz	50 Hz
	16	1xx	800 Kz	6.25 KHz	25 Hz
Autosleep (200 KHz)	1	000	400 Hz	3.2 KHz	12.5 Hz
	2	001	200 Hz	1.6 KHz	6.2 Hz
	4	010	100 Hz	800 Hz	3.1 Hz
	8	011	50 Hz	400 Hz	1.5 Hz
	16	1xx	25 Hz	200 Hz	0.75 Hz

7 Interrupt controller module

Figure 9. Interrupt controller module block diagram



INT_CTRL Interrupt control register

7	6	5	4	3	2	1	0
					POLARITY	TYPE	INT_EN

Address: 0x08

Type: R/W

Reset: 0x00

Description: This register is used to enable control the polarity, edge/level and enabling of the interrupt system.device

[7:3] **RESERVED**

[2] **POLARITY**:
'0' for active low
'1' for active high

[1] **TYPE**:
'0' for level trigger
'1' for edge trigger (pulse width is 200 uS)

[0] **INT_EN**:
'0' to disable all interrupt
'1' to enable all interrupt

INT_EN Interrupt enable register

7	6	5	4	3	2	1	0
GPIO	PWM3	PWM2	PWM1	PWM0	GEN	FIFO	POR

Address: 0x09

Type: R/W

Reset: 0x00

Description: This register is used to enable the interruption from a system related interrupt source to the host. Writing '1' in this register enables the corresponding interrupt event to generate interrupt signal at the INT pin. Note that even if the interrupt is not enabled, an interrupt event will still be reflected in the interrupt status register.

[7] **GPIO**:
One or more level transition in enabled GPIOs

[6] **PWM3:**
Completion of PWM sequence

[5] **PWM2**:
Completion of PWM sequence

[4] **PWM1**:
Completion of PWM sequence

[3] **PWM0**:
Completion of PWM sequence

[2] **GEN**:
System INT (A21, I2A, EOC)

[1] **FIFO**:
Data available in FIFO

[0] **POR**:
Power-on reset

INT_STA Interrupt status register

7	6	5	4	3	2	1	0
GPIO	PWM3	PWM2	PWM1	PWM0	GEN	FIFO	POR

Address: 0x0A

Type: R

Reset: 0x00

Description: This register is used to enable the interruption from a system related interrupt source to the host. Regardless whether the IESYSIOR bits are enabled, the ISSYSIOR bits are still updated. Writing ‘1’ clears a bit in this register. Writing ‘0’ has no effect.

[7] **GPIO**:
One or more level transition in enabled GPIOs

[6] **PWM3:**
Completion of PWM sequence

[5] **PWM2**:
Completion of PWM sequence

[4] **PWM1**:
Completion of PWM sequence

[3] **PWM0**:
Completion of PWM sequence

[2] **GEN**:
System INT (A21, I2A, EOC)

[1] **FIFO**:
Data available in FIFO

[0] **POR**:
Power-on reset

GPIO_INT_EN GPIO interrupt enable registerI

7	6	5	4	3	2	1	0
IEG[x]							

Address: 0x0B, 0x0C

Type: R/W

Reset: 0x00

Description: The GPIO interrupt enable register is used to enable the interruption from a particular GPIO interrupt source to the host. The IEg[7:0] bits and the interrupt enable mask bits correspond to the GPIO[7:0} pins.

[7:0] IEG[7:0]
Interrupt enable GPIO mask (where x = 7 to 0)
Writing a ‘1’ to the IE[x] bit will enable the interruption to the host.

GPIO_INT_STA GPIO interrupt status register

7	6	5	4	3	2	1	0

Address: 0x0D

Type: R/W

Reset: 0x00

Description: The GPIO interrupt status register LSB monitors the status of the interruption from a particular GPIO pin interrupt source to the host. Regardless whether the IEGPIOR bits are enabled or not, the INT_STA_GPIO_LSB bits are still updated. The ISG[7:0] bits are the interrupt status bits correspond to the GPIO[7:0] pins.

[7:0] **ISG[x]**:
Interrupt status GPIO (where x = 7 to 0)
Read:
Interrupt status of the GPIO[x]. Writing ‘1’ clears a bit. Writing ‘0’ has no effect.

8 GPIO controller

A total of 8 GPIOs are available in the STMPE821. The GPIO controller contains the registers that allow the host system to configure each of the pins into either a GPIO, direct output of a TOUCH channel or a PWM output. Unused GPIOs should be configured as outputs to minimize the power consumption.

A group of registers is used to control the exact function of each of the 8 GPIOs. The registers and their respective address is listed in the following table.

Table 8. GPIO controller registers summary map

Address	Register name	Description	Auto-increment
0x10	GPIO_MR_LSB	GPIO monitor pin state register	YES
0x11	GPIO_MR_MSB		
0x12	GPIO_SET_LSB	GPIO set pin state register	YES
0x13	GPIO_SET_MSB		
0x14	GPIO_DIR_LSB	GPIO set pin direction register	YES
0x15	GPIO_DIR_MSB		
0x16	GPIO_FUNCT_LSB	GPIO function register	YES
0x17	GPIO_FUNCT_MSB		

All GPIO registers are named as GPxx, where:

Xxx represents the functional group

For LSB registers:

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

For MSB registers:

7	6	5	4	3	2	1	0
RESERVED							

The function of each bit is shown in the following table:

Table 9. GPIO control bits function

Register name	Function
GPIO monitor pin state	Reading this bit yields the current state of the bit. Writing has no effect.
GPIO set pin state	Writing '1' to this bit causes the corresponding GPIO to go to '1' state Writing '0' to this bit causes the corresponding GPIO to go to '0' state
GPIO set pin direction	'0' sets the corresponding GPIO to input state, and '1' sets it to output state. All bits are '0' on reset. The GPIO must be set as output if the PWM on this pin is to be used.
GPIO function	'1' sets the corresponding GPIO to function as GPIO/PWM, and '0' sets it to touchkey direct output mode. For GPIO 0-3, if the GPIO function is set to GPIO/PWM mode and the AF bits in the PWM master enable register is enabled, the corresponding GPIO will function as PWM output.

9 Capacitive touch module registers

Table 10. TOUCH_FIFO summary table

Address	Function
0x18	FIFO-0, LSB
0x19	FIFO-0, MSB
0x1A	FIFO-1, LSB
0x1B	FIFO-1, MSB
0x1C	FIFO-2, LSB
0x1D	FIFO-2, MSB
0x1E	FIFO-3, LSB
0x1F	FIFO-3, MSB

TOUCH_FIFO Touch FIFO

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

Address: 0x19, 0x18

Type: R

Reset: 0x00

Description: TOUCH_FIFO is the access port for the internal 4-level FIFO used for buffering the touch events. While it is possible to access each bytes in the data structure directly, it is recommended that the FIFO is accessed only via the 0x18 address.

The FIFO must be accessed in multiples of 2 bytes (LSB, MSB). For STMPE821, MSB is reserved and LSB contains a snapshot of the recent touch event. The FIFO must be accessed in multiples of 2 bytes (LSB, MSB). For STMPE821, MSB is reserved and LSB contains a snapshot of the recent touch event.

Where Tn is touch status of touch sensing channel n.

FEATURE_SELECT Feature select

7	6	5	4	3	2	1	0
RESERVED				AFS3	AFS2	AFS1	Filter EN

Address: 0x20

Type: R/W

Reset: 0x04

Description: Controls AFS (advanced filtering system and second level filtering feature

[7:4] **RESERVED**

[3] **AFS3**:
Write '1' to enable AFS mode 3

[2] **AFS2**:
Write '1' to enable AFS mode 2

[1] **AFS1**:
Write '1' to enable AFS mode 1

[0] **Filter EN**:
Write '1' to enable filter

ETC_WAIT Wait time setting

7	6	5	4	3	2	1	0
ETC_WAIT[7:0]							

Address: 0x21

Type: R/W

Reset: 0x27

Description: Sets the wait time between the calibration and the last button touch

[7:0] **ETC_WAIT[7:0]**:
ETC wait time = ETC_Wait[7:0] *64 + sensor clock period

A "non-touch" condition must persist for this wait time, before an ETC operation is carried out.

Range: 800 mS - 12.8 S

CAL_INTERVAL Calibration interval

7	6	5	4	3	2	1	0
CAL_INTERVAL							

Address: 0x22

Type: R/W

Reset: 0x30

Description: Calibration interval

[7:0] **CALIBRATION INTERVAL**:
Interval between calibration = Calibration Interval [7:0] * sensor clock period * 50

Range: 625 mS - 10 S

INTEGRATION TIME Integration time

7	6	5	4	3	2	1	0
INTEGRATION_TIME[7:0]							

Address: 0x23

Type: R/W

Reset: 0x0F

Description: Integration time

[7:0] Integration time in AFS mode

Total period of integration = sensor clock period * Integration Time [7:0]

50uS - 800uS

CTRL Control

7	6	5	4	3	2	1	0
RESERVED				F2A	HDC_U	HDC_C	HOLD

Address: 0x25

Type: R/W

Reset: 0x00

Description: Control

[7:4] 0x90

[3] **F2A**:
Write '1' to force device to remain in ACTIVE state at all times

[2] **HDC_U**:
Write '1' to perform unconditional host driven calibration.
Cleared to '0' when calibration is completed

Only applicable HOLD is '1'

[1] **HDC_C**:
Write '1' to perform conditional host driven calibration.
Calibration is performed if and only if no touch is detected.
Cleared to '0' when calibration is completed

Only applicable HOLD is '1'

[0] **HOLD**:
'0' to enable ETC
'1' to disable ETC

INT_MASK Interrupt mask

7	6	5	4	3	2	1	0
RESERVED				EOC	I2A	A2I	RESERVED

Address: 0x26

Type: R/W

Reset: 0x08

Description: Writing '1' to this register disables the corresponding interrupt source.

[7:4] RESERVED

[3] **EOC**:
End of calibration
This interrupt occurs on both automatic and forced calibration

[2] **I2A**:
SLEEP to Active transition

[1] **A2I**:
Active to SLEEP transition

[0] **RESERVED**

INT_CLR Interrupt clear

7	6	5	4	3	2	1	0
RESERVED				EOC	I2A	A2I	RESERVED

Address: 0x27

Type: R/W

Reset: 0x00

Description: Writing '1' to this register clears the corresponding interrupt source in INT_PENDING register.

[7:4] 0x90

[3] **EOC**:
End of calibration
This interrupt occurs on both automatic and forced calibration

[2] **I2A**:
SLEEP to Active transition

[1] **A2I**:
Active to SLEEP transition

[0] **RESERVED**

FILTER_PERIOD Filter period

7	6	5	4	3	2	1	0
FILTER_COUNT							

Address: 0x28

Type: R/W

Reset: 0x00

Description: Filter period.

[7:0] **FILTER_COUNT**:
Additional filter to stabilize touch output in AFS mode.

AFS touch output is monitored for Filter Count [7:0] times every integration time. For each time a "touch status" is detected, an internal "Filter Counter" is incremented once. This counter value is then compared with Filter Threshold (register 0x3E)

FILTER_THRESHOLD Filter threshold

7	6	5	4	3	2	1	0
FILTER_THRESHOLD							

Address: 0x29

Type: R/W

Reset: 0x00

Description: Filter threshold.

[7:0] **FILTER_THRESHOLD**:
An internal "Filter Counter" is compared with Filter Threshold [7:0] to determine if a valid touch has occurred.

REFERENCE_DELAY Reference delay

7	6	5	4	3	2	1	0
RESERVED	REFERENCE_DELAY						

Address: 0x2A

Type: R/W

Reset: 0x00

Description: Shifting of capacitive sensor dynamic range. The capacitance value set into this register is in effect, equivalent to capacitor connected to the S_Ref pin.

[7] RESERVED

[6:0] **REFERENCE_DELAY**:
Valid range = 0-127
Each step represents capacitance value of 0.06 pF
Warm reset is required after this value is updated

TVR Touch variance setting

7	6	5	4	3	2	1	0
RESERVED	TVR						

Address: 0X30 - 0x3B

Type: R/W

Reset: 0x08

Description: Touch variance setting.

[7] RESERVED

[6:0] **TVR**:
Setting TVR between 0-99

A high TVR value decreases sensitivity of the sensor, but increasing its tolerance to ambient noise

A small TVR value increases the sensitivity.

EVR Enviromental variance

7	6	5	4	3	2	1	0
RESERVED	TVR						

Address: 0x40

Type: R/W

Reset: 0x04

Description: Enviromental variance setting.

[7] RESERVED

[6] **EVR**:
EVR is used to detect "Non-Touch" condition

STRENGTH_THRESHOLD Strength threshold

7	6	5	4	3	2	1	0
STRENGTH_THRESHOLD							

Address: 0x50 - 0x5B

Type: R/W

Reset: 0x01

Description: Strength threshold.

[7:0] **STRENGTH_THRESHOLD**:
Setting threshold to be used in AFS mode to determine valid touch

STRENGTH Strength

7	6	5	4	3	2	1	0
STRENGTH							

Address: 0x60 - 0x67

Type: R

Reset: 0x00

Description: The number of times where a sense capacitance exceeds the calibrated reference impedance

[7:0] **STRENGTH**:
Read-only field
Counts the number of times a sensed impedance exceeds calibrated reference impedance over and integration time. Maximum strength equals Integration Time [7:0]

CALIBRATED_IMPEDANCE Calibrated impedance

7	6	5	4	3	2	1	0
CAL_IMPEDANCE							

Address: 0x70 - 0x77

Type: R

Reset: 0x00

Description: Calibrated impedance is an integral reference value maintained by the device.

[7:0] **CALIBRATED IMPEDANCE**:
Calibrated reference impedance

IMPEDANCE Impedance

7	6	5	4	3	2	1	0
IMPEDANCE							

Address: 0x80 - 0x87

Type: R

Reset: 0x00

Description: Impedance is the instantaneous impedance value seen at the input pin of eac cap. sensing pin.

[7:0] **IMPEDANCE**:
Currently sensed impedance

TOUCH_BYTE_L Touch byte L

7	6	5	4	3	2	1	0
TOUCH							

Address: 0x90

Type: R

Reset: 0x00

Description: Touch status of capacitive channel 0 - 7.

[7:0] **TOUCH**:
Reads '1' if the corresponding capacitance sensing channel reads a valid TOUCH

TOUCH_BYTE_H Touch byte H

7	6	5	4	3	2	1	0
RESERVED							

Address: 0x91

Type: R

Reset: 0x00

Description: Reserved.

[7:0] RESERVED:

INT_PENDING Interrupt pending

7	6	5	4	3	2	1	0
RESERVED				EOC	I2A	A21	RESERVED

Address: 0x92

Type: R/W

Reset: 0x00

Description: Reflects the status of each interrupt source.

[7:4] RESERVED

[3] **EOC**:
End of calibration

[2] **I2A**:
SLEEP to active transition

[1] **A21**:
Active to SLEEP transition

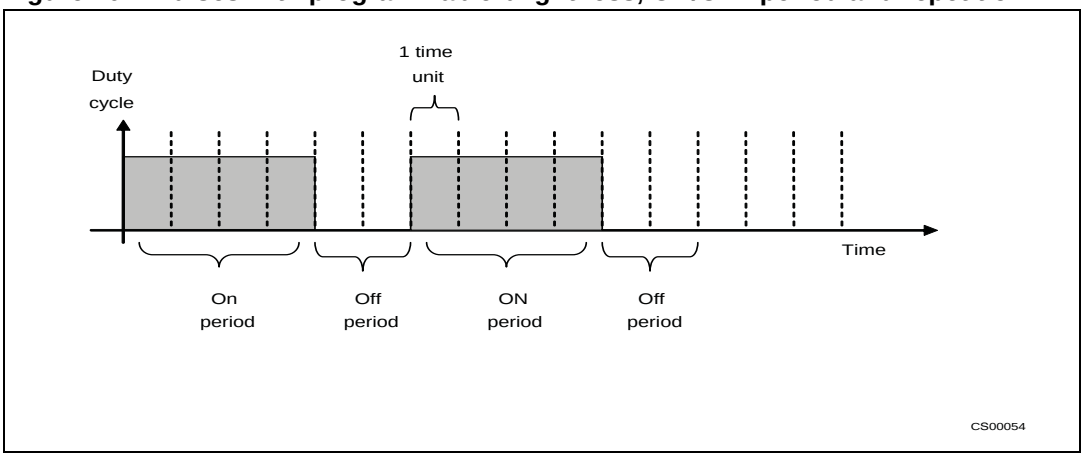
[0] **RESERVED**

10 Basic PWM controller

The advanced PWM allows complex brightness and blinking control of a LED. The basic PWM controller allows simpler brightness control and basic blinking patterns. The STMPE821 is fitted with a 4-channel basic PWM controller.

The PWM controllers outputs are connected to the GPIO 0-3. In order to activate the PWM channels, the alternate function bits in the master enable register must be set to '1'. The PWM controllers are capable of generating the following brightness patterns:

Figure 10. Pulses with programmable brightness, ON/OFF period and repetition



On period = period 0[1:0] * time unit [3:0]

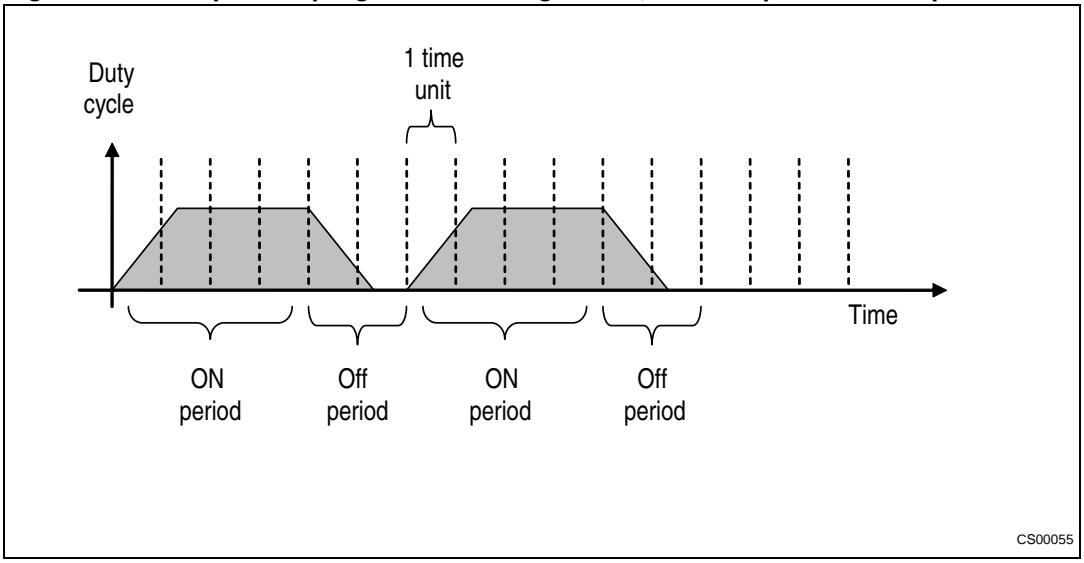
Off period = period 1[1:0] * time unit [3:0]

Duty cycle during “on period” = brightness [7:4]

Number of cycles = repetition [3:0]

Ramp mode is disabled

Figure 11. Ramps with programmable brightness, ON/OFF period and repetition



“On” period = period 0[1:0] * time unit [3:0]

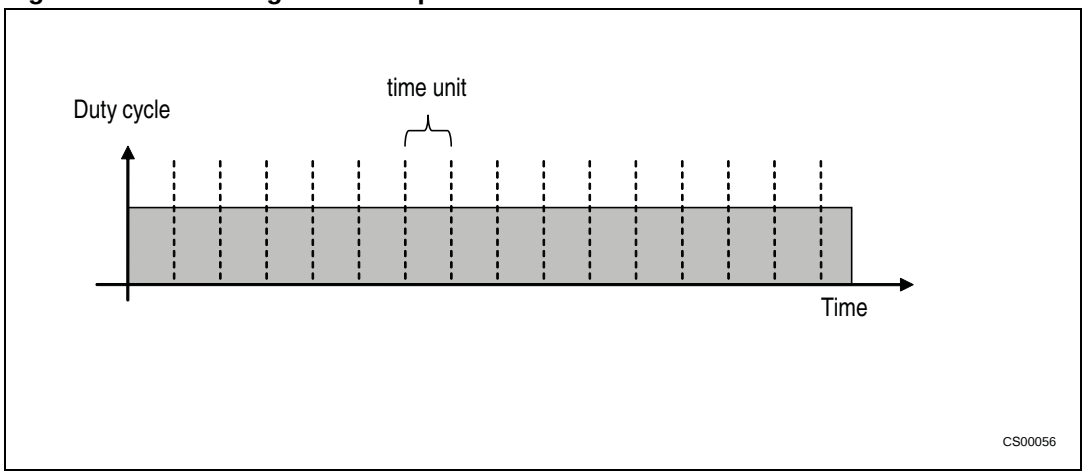
“Off” period = period 1[1:0] * time unit [3:0]

Duty cycle during “on” period = brightness [7:4]

Number of cycles = repetition [3:0]

Ramp up rate is programmable.

Figure 12. Fixed brightness output



“On” period = period 0[1:0] * time unit [3:0]

Off period = don't care

Duty cycle during “on” period = brightness [7:4]

Number of cycles = repetition [3:0] = 0 (means infinite repetition)

10.1 PWM function register map

Table 11. PWM function register map summary table

Register name	Description	Auto-increment (during sequential R/W)
PWM_OFF_OUTPUT	Set the output level when PWM is disabled	Yes
MASTER_EN	Enables/disables individual basic PWM channels	Yes
PWM0_SET	PWM 0 setup	Yes
PWM0_CTRL	PWM 0 control	Yes
PWM0_RAMP_RATE	PWM 0 ramp rate	Yes
PWM1_SET	PWM 1 setup	Yes
PWM1_CTRL	PWM 1 control	Yes
RAMP1_RATE	PWM 1 ramp rate	Yes
PWM2_SET	PWM 2 setup	Yes
PWM2_CTRL	PWM 2 control	Yes
RAMP2_RATE	PWM 2 ramp rate	Yes
PWM3_SET	PWM 3 setup	Yes
PWM3_CTRL	PWM 3 control	Yes
PWM3_RATE	PWM 3 ramp rate	Yes

MASTER_EN Master enabler

7	6	5	4	3	2	1	0
AF3	AF2	AF2	AF0	EN3	EN2	EN1	EN0

Address: 0xA1

Type: R/W

Reset: 0x00

Description: Write ‘1’ to select PWM function on the corresponding channel.

[7:4] AF3:0

[3:0] **OUT3:0**:
Default is '0'.
Write ‘1’ to used the corresponding PWM channel must be diabled for the controlling registers to be accessed.

PWM_OFF_OUTPUT PWM group control register

7	6	5	4	3	2	1	0
				OUT3	OUT2	OUT1	OUT0

Address: 0xA0

Type: R/W

Reset: 0x00

Description: PWM group control register.

[7:4] RESERVED

[3:0] **OUT3:0**:
Default is '0'
'1' - PWM channel outputs '1' when disabled
'0' - PWM channel outputs '0' when disabled

RAMP_RATE Ramp rate register

7	6	5	4	3	2	1	0
RESERVED		RAMP_DOWN			RAMP_UP		

Address: 0xB2

Type: R/W

Reset: 0x00

Description: Ramp rate register.

[7:6] RESERVED

[5:3] **RAMP_DOWN [2:0]**:
'000' = 1/4 of time unit per brightness level change
'001' = 1/8 of time unit per brightness level change
'010' = 1/16 of time unit per brightness level change
'011' = 1/32 of time unit per brightness level change
'100' = 1/64 of time unit per brightness level change
'101' = 1/128 of time unit per brightness level change
'110' = reserved
'111' = reserved

[2:0] **RAMP_UP [2:0]**:
'000' = 1/4 of time unit per brightness level change
'001' = 1/8 of time unit per brightness level change
'010' = 1/16 of time unit per brightness level change
'011' = 1/32 of time unit per brightness level change
'100' = 1/64 of time unit per brightness level change
'101' = 1/128 of time unit per brightness level change
'110' = reserved
'111' = reserved

PWM_n_SETUP PWM_n setup register (n=0-3)

7	6	5	4	3	2	1	0
BRIGHTNESS				TIMING			

Address: 0xB0

Type: R/W

Reset: 0x00

Description: PWM setup register.

[7:4] BRIGHTNESS:

This defines the duty cycle during the ON period of the PWM channel output which in turn determines the brightness level of the LED that the PWM output drives.

0000: Duty cycle ratio 1:15 (6.25%, minimum brightness)
0001: Duty cycle ratio 2:14 (12.50%)
0010: Duty cycle ratio 3:13 (18.75%)
0011: Duty cycle ratio 4:12 (25.00%)
0100: Duty cycle ratio 5:11 (31.25%)
0101: Duty cycle ratio 6:10 (37.50%)
0110: Duty cycle ratio 7: 9 (43.75%)
0111: Duty cycle ratio 8: 8 (50.00%)
1000: Duty cycle ratio 9: 7 (56.25%)
1001: Duty cycle ratio 10: 6 (62.50%)
1010: Duty cycle ratio 11: 5 (68.75%)
1011: Duty cycle ratio 12: 4 (75.00%)
1100: Duty cycle ratio 13: 3 (81.25%)
1101: Duty cycle ratio 14: 2 (87.50%)
1110: Duty cycle ratio 15: 1 (93.75%)
1111: Duty cycle ratio 16: 0 (100.00%, maximum brightness)

[3:1] **TIMING**[3:0] is the time unit from which the duration of the ON period and OFF period is defined in:

"000" = 20 mS
"001" = 40 mS
"010" = 80 mS
"011" = 160 mS
"100" = 320 mS
"101" = 640 mS
"110" = 1280 mS
"111" = 2560 mS

[0] Write '1' to activate ramp mode

PWM_CTRL_n PWM control register n=0-3

7	6	5	4	3	2	1	0
PERIOD_0		PERIOD_1		REPETITION			FRAME_ORDER

Address: 0xB1, 0xB5, 0xB9, 0xBD

Type: R/W

Reset: 0x00

Description: This register controls the sequence and repetition of blinking.

[7:6] **PERIOD_0**:

This defines the ON period time which is when the PWM channel output is toggling. The time unit is as defined in the TIMING bits of the respective TIMING_SETUP registers:

00: 1 time unit

01: 2 time unit

10: 3 time unit

11: 4 time unit

[5:4] **PERIOD_1**:

This defines the OFF period time which is when the PWM channel output is low, that is, not toggling. The time unit is as defined in the TIMING bits of the respective TIMING_SETUP registers:

00: 0 time unit. This means that there is no OFF period but only ON period, that is, the PWM channel output will always be toggling.

01: 1 time unit

10: 2 time unit

11: 3 time unit

[3:1] **REPETITION**:

This defines the number of repetition of pairs of PERIOD_0 and PERIOD_1.

000: infinite repetition.

001: execute only one pair.

010: execute 2 pairs

011: execute 3 pairs

100: execute 4 pairs

101: execute 5 pairs

110: execute 6 pairs

111: execute 7 pairs

[0] **FRAME_ORDER**:

For PWM mode, this defines which frame, PERIOD_0 or PERIOD_1 comes first.

0: PERIOD_0 is outputted first then PERIOD_1.

1: PERIOD_1 is outputted first then PERIOD_0.

10.2 Interrupt on basic PWM controller

The basic PWM controller can be programmed to generate interrupts on completion of the blinking sequence.

a) Each basic PWM controller has its own bit in interrupt the enable/status registers.

b) If enabled, completion in any of the PWM controller triggers interrupts. No interrupt is generated if infinite repetition is set.

11 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{CC}	Power supply			2.5	V
V_{IO}	GPIO supply voltage			6.0	V
V_{ESD}	ESD protection on each GPIO/touch pin			8	kV

12 Electrical specifications

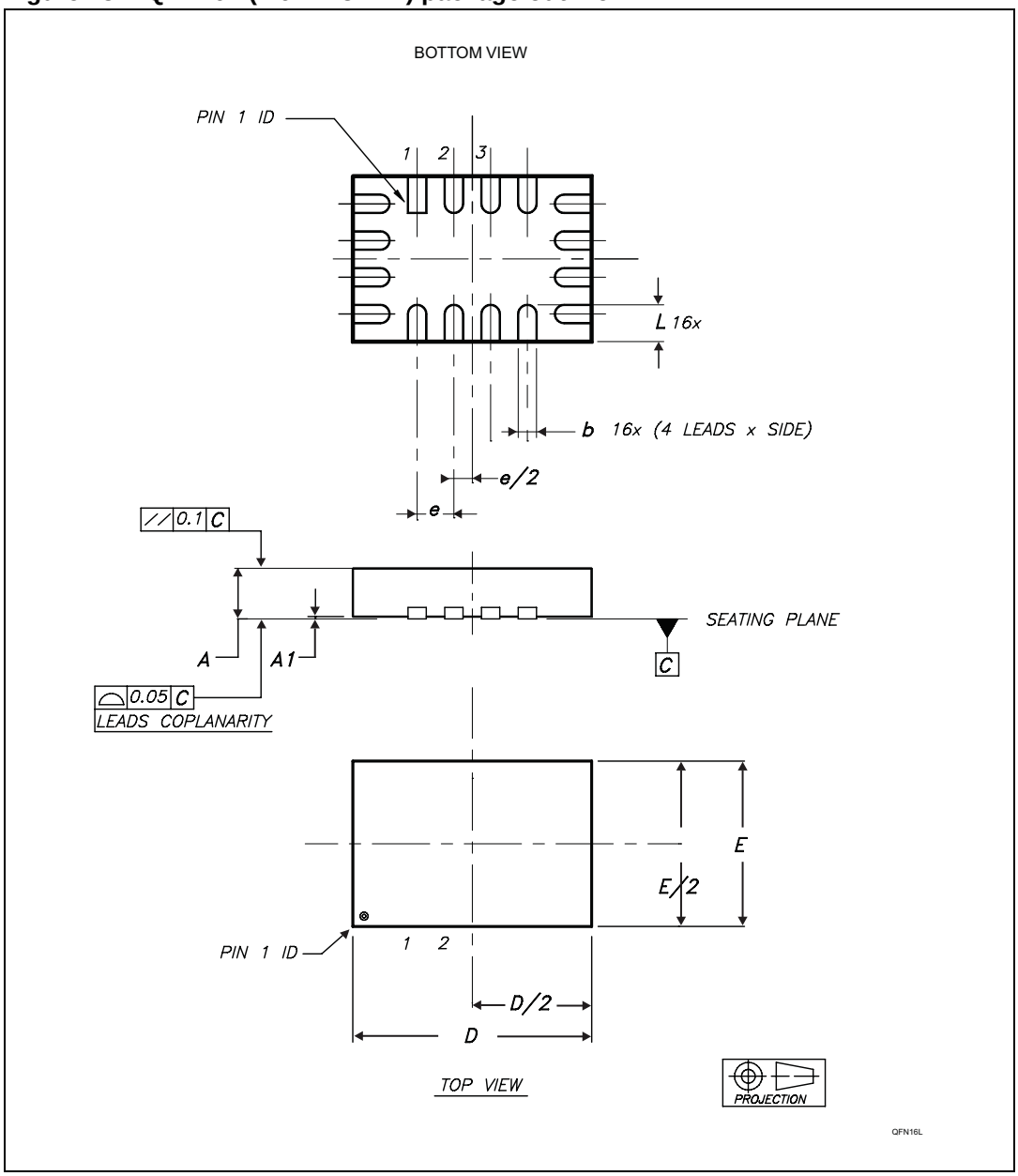
Table 13. DC electrical characteristics (-40 –85 °C unless otherwise stated))

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{CC}	Core supply voltage		1.65	–	1.95	V
V_{IO}	IO supply voltage		1.65	–	5.5	V
I_{active}	Active current	5% touch activity		42	63	µA
I_{active}	Active current	10% touch activity		60	90	µA
I_{active}	Active current	100% touch activity		350	550	µA
I_{sleep}	Sleep current			25	40	µA
$I_{hibernate}$	Hibernate current			4	7	µA
V_{IL}	Input voltage low state (reset/I^2C)	V_{CC} = 1.8 V	-0.3 V		0.35 V_{CC}	V
V_{IH}	Input voltage high state (reset/I^2C)	V_{CC} = 1.8 V	0.65 V_{CC}		V_{CC}+0.3 V	V
V_{IL}	Input voltage low state (GPIO)	V_{IO} = 1.8 –5.0 V	-0.3 V_{IO}		0.35 V_{IO}	V
V_{IH}	Input voltage high state (GPIO)	V_{IO} = 1.8 –5.0 V	0.65 V_{IO}		V_{IO}+0.3 V	V
V_{OL}	Output voltage low state (GPIO)	V_{IO} = 1.8 V, I_{OL} = 4 mA	-0.3 V		0.25 V_{IO}	V
V_{OH}	Output voltage high state (GPIO)	V_{IO} = 1.8 V, I_{OL} = 4 mA	0.75 V_{IO}		V_{IO}+0.3 V	V
V_{OL}	Output voltage low state (GPIO)	V_{IO} = 3.3 –5.0 V, I_{OL} = 8 mA	-0.3 V		0.25 V_{IO}	V
V_{OH}	Output voltage high state (GPIO)	V_{IO} = 3.3 –5.0 V, I_{OL} = 8 mA	0.75 V_{IO}		V_{IO}+0.3 V	V
$I_{LEAKAGE}$	Input leakage current	V_{IN} = 5.5 V, V_{IO} = 5.5 V All GPIOs		0.05	0.5	µA

13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 13. QFN16L (2.6 x 1.8 mm) package outline

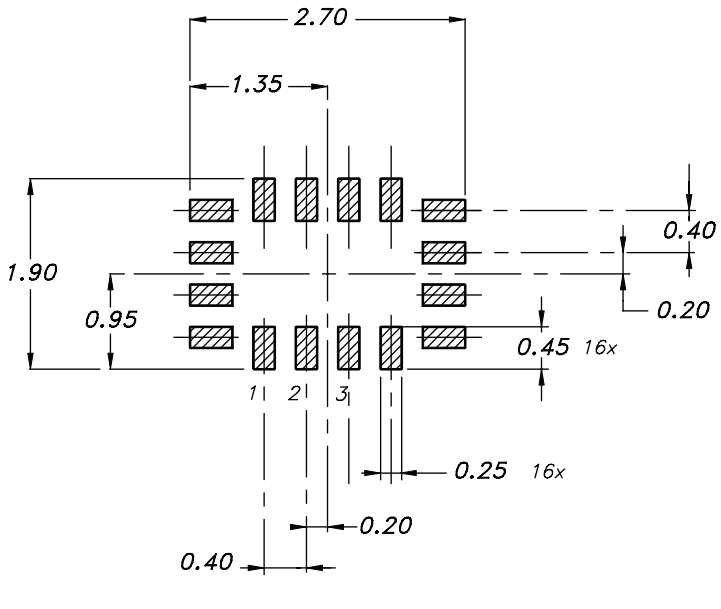


1. Drawing not to scale.
2. Dimensions are in millimeters.

Table 14. QFN16L (2.6 x 1.8 mm) mechanical data

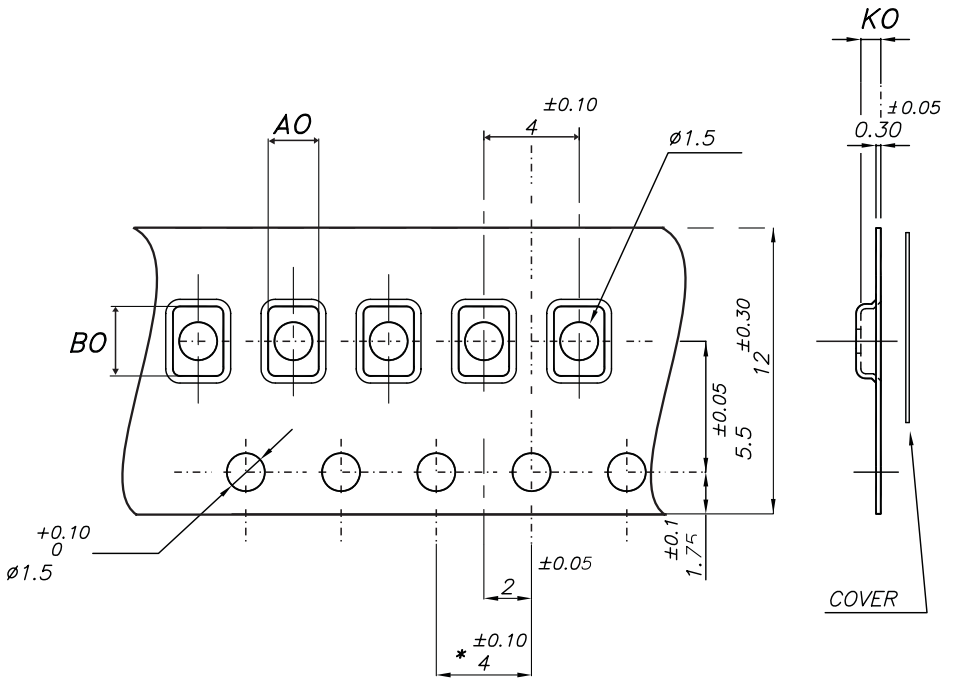
Symbol	millimeters		
	Typ	Min	Max
A	0.55	0.45	0.60
A1	0.02	0	0.05
b	0.20	0.15	0.25
D	2.60	2.50	2.70
E	1.80	1.70	1.90
e	0.40		
L	0.40	0.35	0.45

Figure 14. QFN16L (2.6 x 1.8 mm) footprint recommentations



1. Drawing not to scale.
2. Dimensions are in millimeters.

Figure 15. QFN16L (2.6 x 1.8 mm) carrier tape

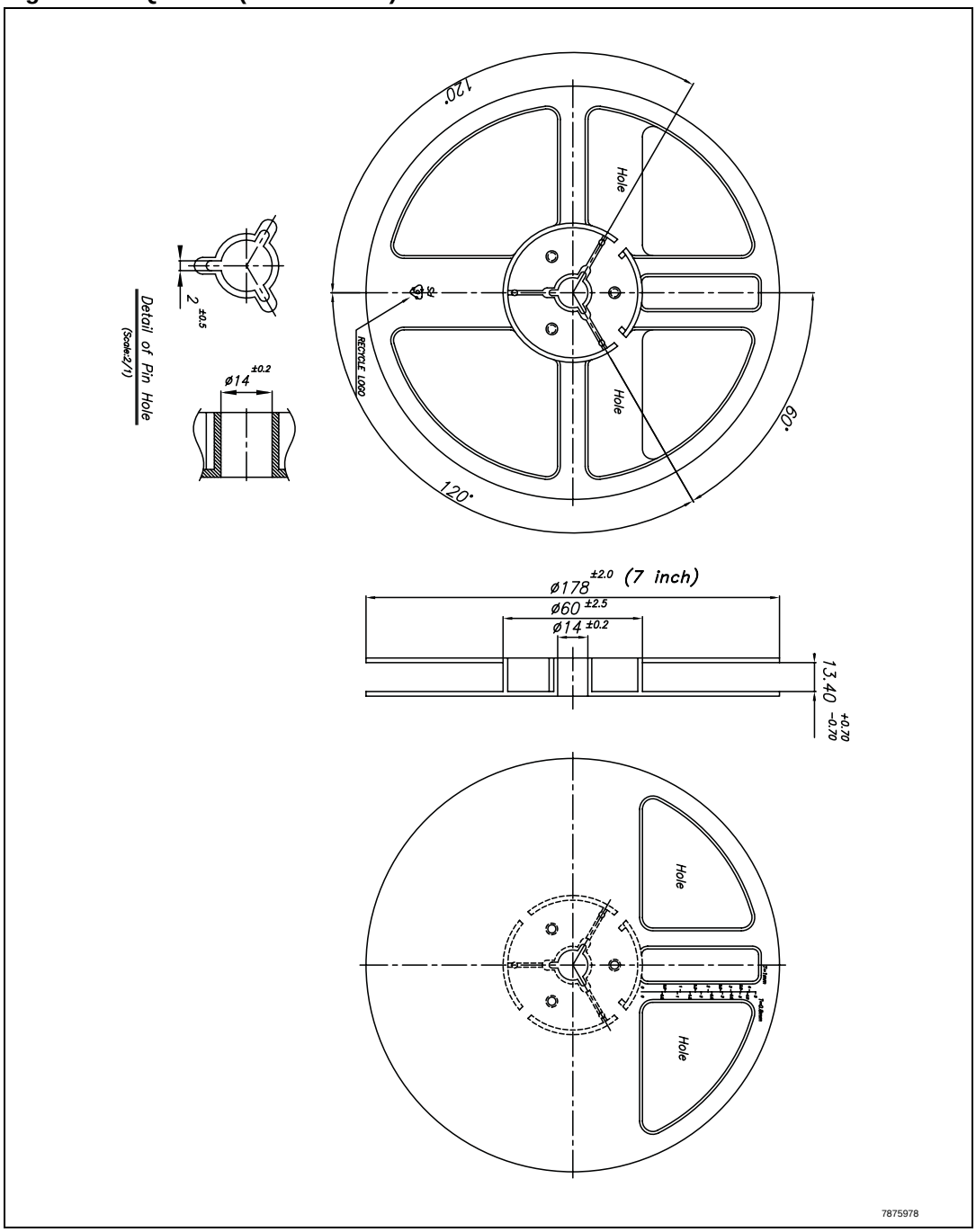


AO	2.10 ±0.05
BO	2.90 ±0.05
KO	0.75 ±0.05

* 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20

785978-J

Figure 16. QFN16L (2.6 x 1.8 mm) reel information



1. Drawing not to scale.
2. Dimensions are in millimeters

14 Revision history

Table 15. Document revision history

Date	Revision	Changes
26-Feb-2008	1	Initial release.
10-Jun-2008	2	Modified: operating voltage range so as to included support for 5.5 V, *Section 1.3 on page 6*, *Figure 5 on page 9*, *Section 4 on page 11*, *Section 5 on page 13*, *Section 8 on page 23*, Added: PWM_CTRL_n register description and $I_{LEAKAGE}$ value in *Table 13 on page 49*

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