



# ESDA6V1U1

Application Specific Discretes  
A.S.D.

## TRANSIL ARRAY FOR ESD PROTECTION

### APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- COMPUTERS
- PRINTERS
- COMMUNICATION SYSTEMS
- GSM HANDSETS AND ACCESSORIES
- CAR RADIO

It is particularly recommended for parallel port protection where the line interface withstands only 2 kV ESD surge.

### FEATURES

- 6 UNIDIRECTIONAL TRANSIL FUNCTIONS
- LOW LEAKAGE CURRENT:  $I_R \text{ max.} < 2 \mu\text{A}$
- 200 W PEAK PULSE POWER (8/20  $\mu\text{s}$ )

### DESCRIPTION

The ESDA6V1U1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

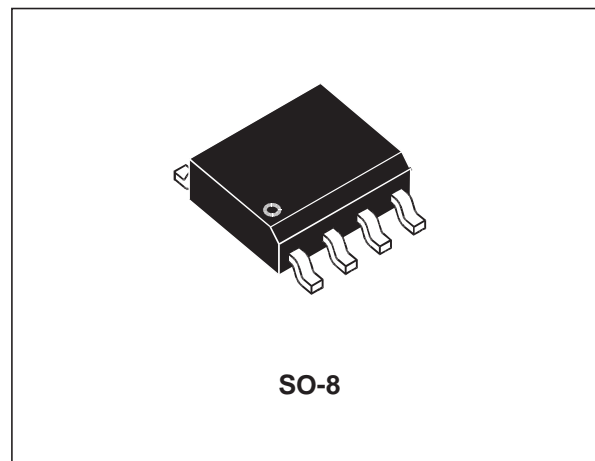
### BENEFITS

High ESD protection level : up to 25 kV  
High integration  
Suitable for high density boards

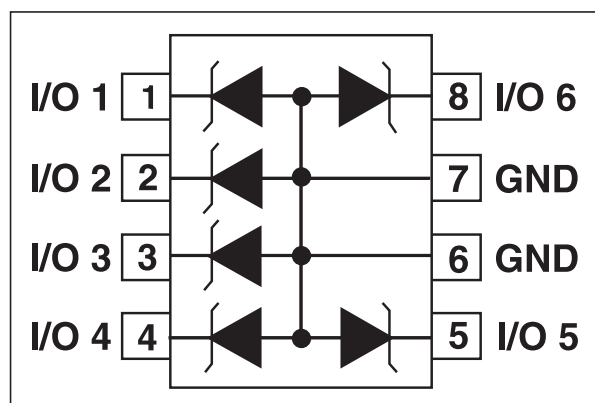
### COMPLIES WITH THE FOLLOWING STANDARDS :

IEC61000-4-2 : level 4

MIL STD 883C-Method 3015-6 : class3  
(human body model)



### FUNCTIONAL DIAGRAM



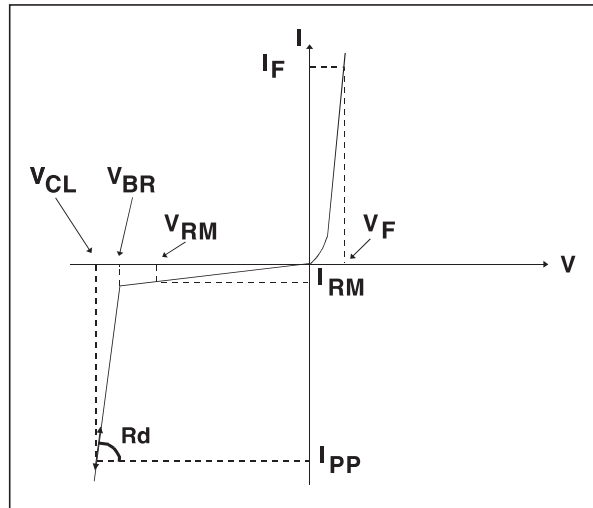
# ESDA6V1U1

## ABSOLUTE MAXIMUM RATINGS (T<sub>amb</sub> = 25°C)

Symbol	Parameter	Value	Unit
V <sub>PP</sub>	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P <sub>PP</sub>	Peak pulse power (8/20μs)	200	W
T <sub>stg</sub> T <sub>j</sub>	Storage temperature range Maximum junction temperature	- 55 to + 150 125	°C °C
T <sub>L</sub>	Maximum lead temperature for soldering during 10s	260	°C

## ELECTRICAL CHARACTERISTICS (T<sub>amb</sub> = 25°C)

Symbol	Parameter
V <sub>RM</sub>	Stand-off voltage
V <sub>BR</sub>	Breakdown voltage
V <sub>CL</sub>	Clamping voltage
I <sub>RM</sub>	Leakage current
I <sub>PP</sub>	Peak pulse current
α <sub>T</sub>	Voltage temperature coefficient
C	Capacitance
R <sub>d</sub>	Dynamic resistance
V <sub>F</sub>	Forward voltage drop



Types	V <sub>BR</sub> @		I <sub>R</sub>	I <sub>RM</sub> @ V <sub>RM</sub>		R <sub>d</sub> typ. note 1	α <sub>T</sub> max. note 2	C typ. 0V bias	V <sub>F</sub> @ I <sub>F</sub>	
	min.	max.		max.					max.	
	V	V	mA	μA	V	Ω	10 <sup>-4</sup> /°C	pF		
ESDA6V1U1	6.1	7.2	1	2	5	0.5	6	100	1.5	200

note 1 : Square pulse, I<sub>pp</sub> = 25A, t<sub>p</sub> = 2.5μs.

note 2 : Δ V<sub>BR</sub> = α<sub>T</sub> \* (T<sub>amb</sub> - 25°C) \* V<sub>BR</sub> (25°C)

## CALCULATION OF THE CLAMPING VOLTAGE

### USE OF THE DYNAMIC RESISTANCE

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage  $V_{CL}$ . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

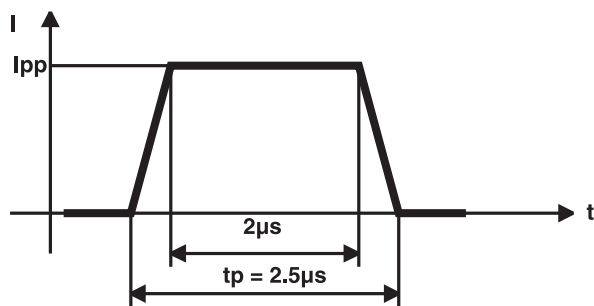
$$V_{CL} = V_{BR} + R_d I_{PP}$$

Where  $I_{PP}$  is the peak current through the ESDA cell.

As the value of the dynamic resistance remains stable for a surge duration lower than  $20\mu s$ , the  $2.5\mu s$  rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of  $R_d$ .

### DYNAMIC RESISTANCE MEASUREMENT

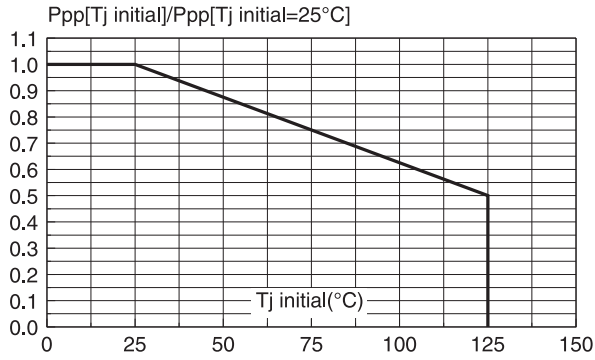
The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical  $8/20\mu s$  and  $10/1000\mu s$  surges.



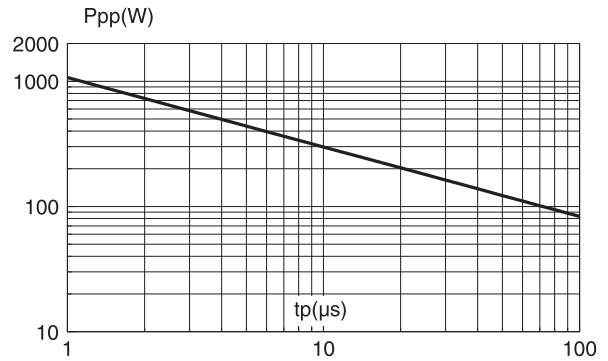
$2.5\mu s$  duration measurement wave.

# ESDA6V1U1

**Fig. 1 :** Peak power dissipation versus initial junction temperature.

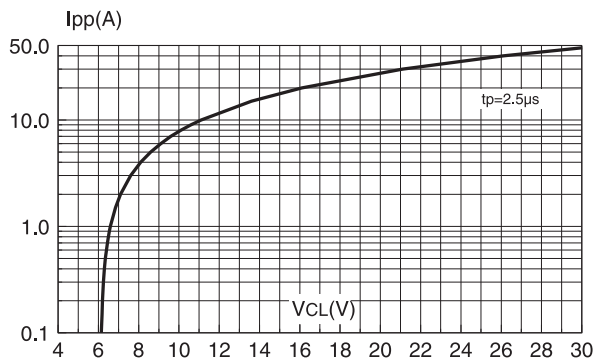


**Fig. 2 :** Peak pulse power versus exponential pulse duration ( $T_j \text{ initial} = 25^\circ\text{C}$ ).

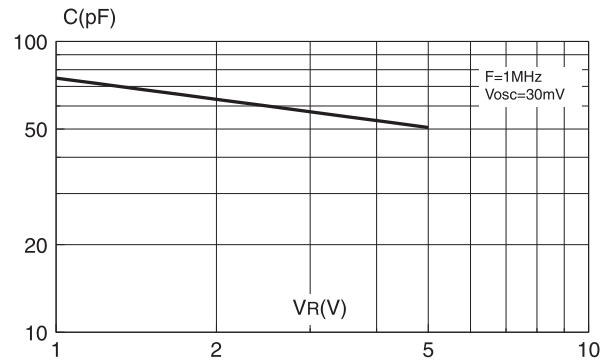


**Fig. 3 :** Clamping voltage versus peak pulse current ( $T_j \text{ initial} = 25^\circ\text{C}$ ).

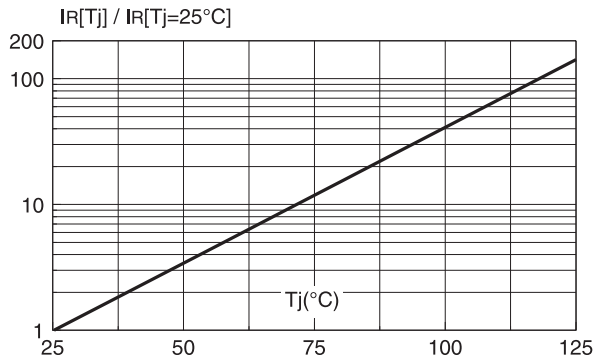
Rectangular waveform  $t_p = 2.5 \mu\text{s}$ .



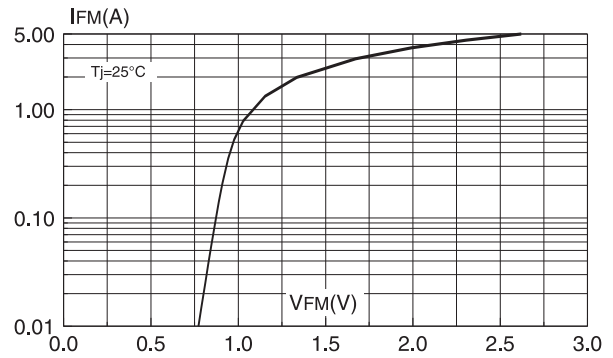
**Fig. 4 :** Capacitance versus reverse applied voltage (typical values).

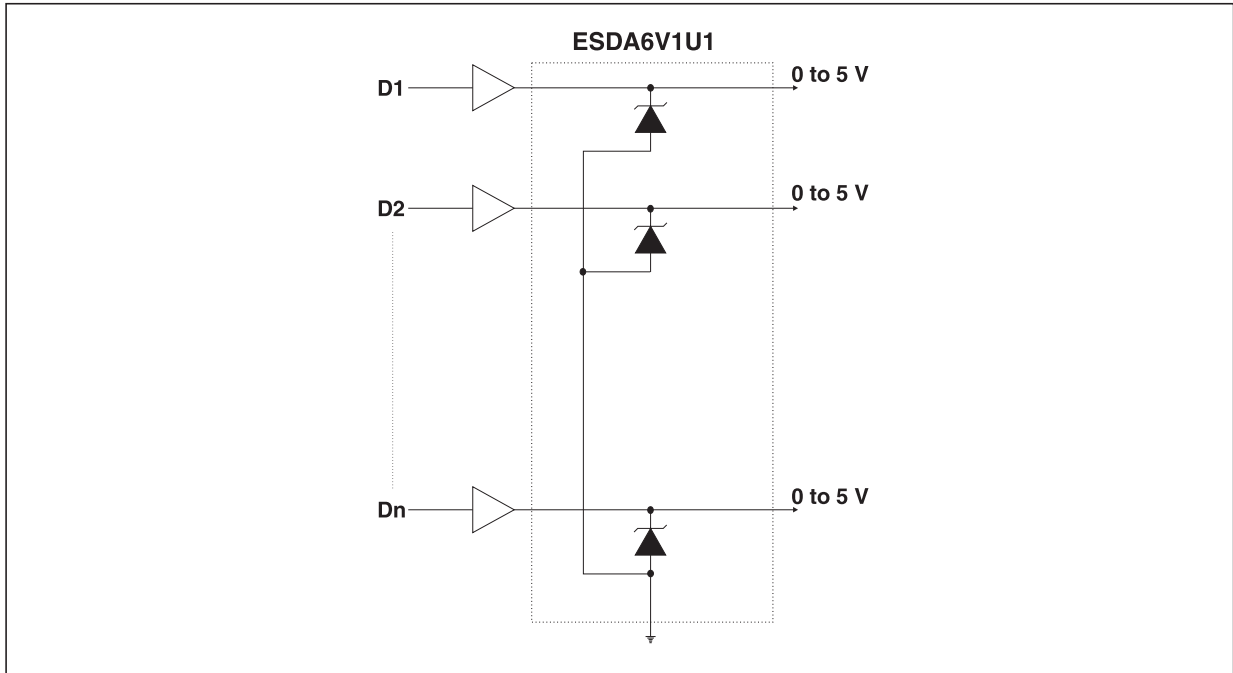


**Fig. 5 :** Relative variation of leakage current versus junction temperature (typical values).

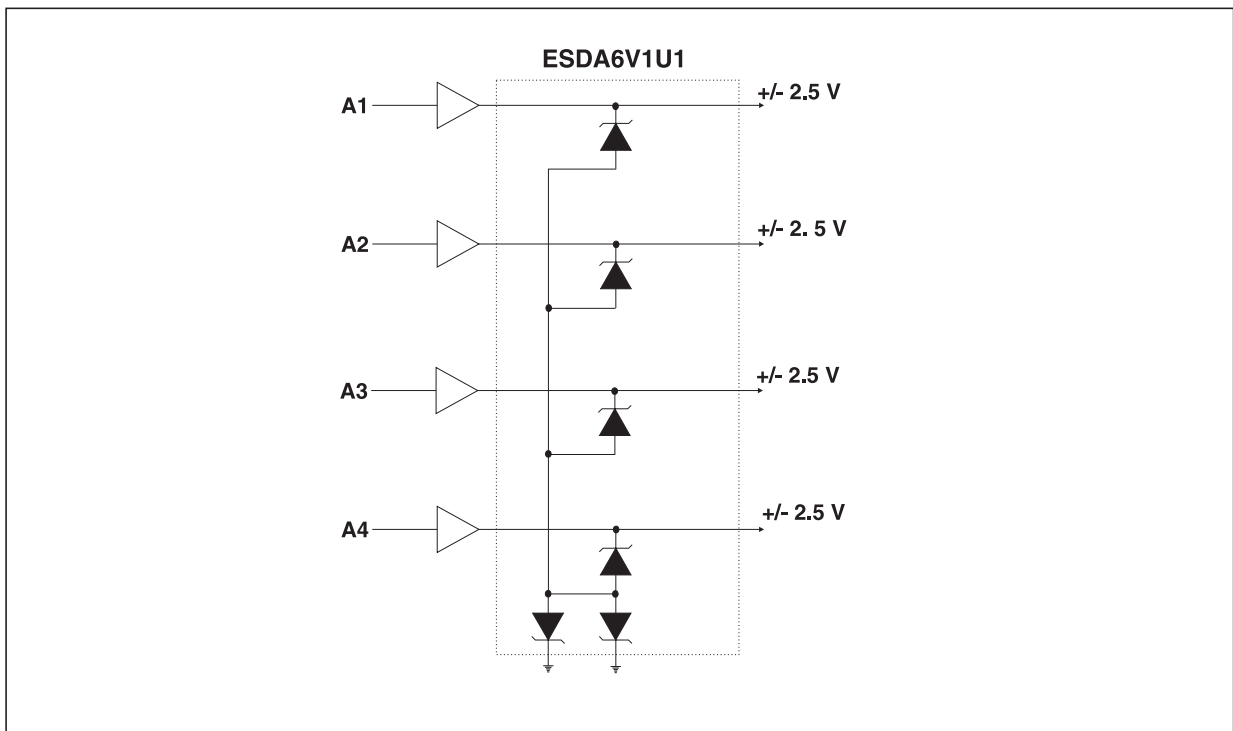


**Fig. 6 :** Peak forward voltage drop versus peak forward current (typical values).



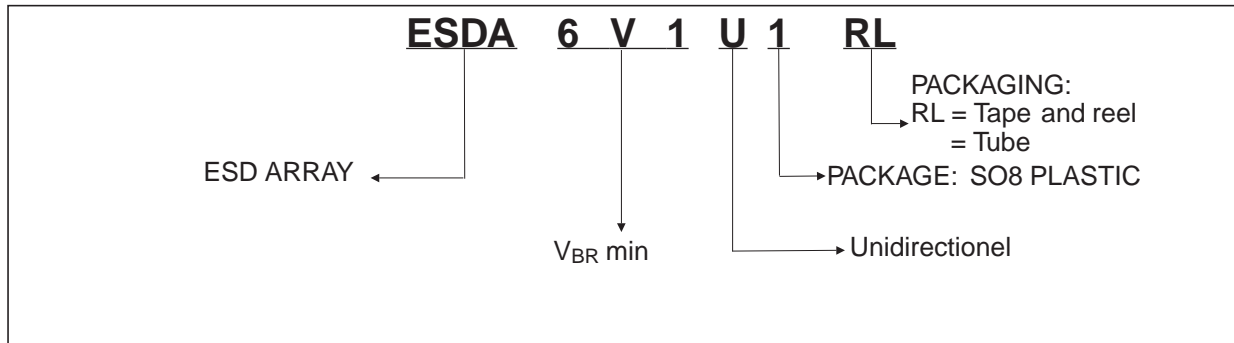
**APPLICATION EXAMPLE :** Protection of logic-level signals.**APPLICATION EXAMPLE :** Protection of symmetrical signals.

**Note :** Capacitance value between any I/O pin and Ground is divided by 2.



# ESDA6V1U1

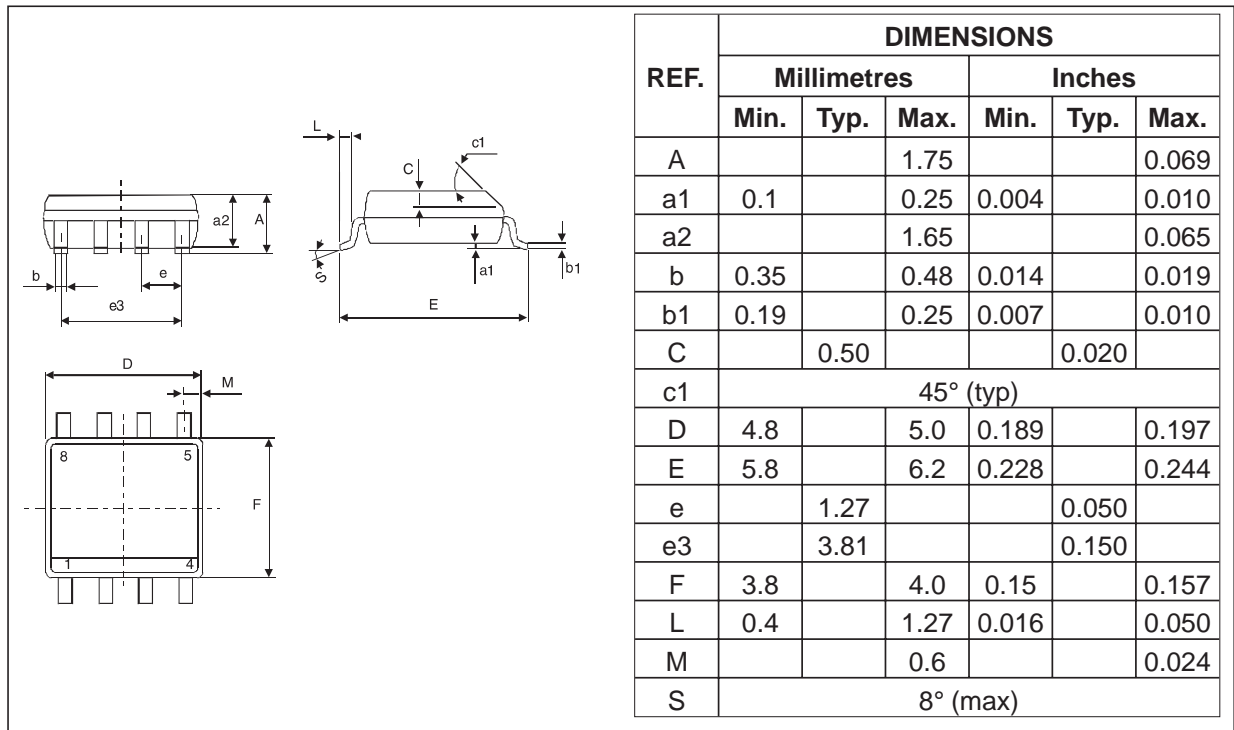
## ORDER CODE



**MARKING** : Logo, Date Code, E6V1U1

## PACKAGE MECHANICAL DATA

SO-8 Plastic



**Packaging** : Preferred packaging is tape and reel.

**Weight** : 0.08g.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics  
 © 2002 STMicroelectronics - Printed in Italy - All rights reserved.  
 STMicroelectronics GROUP OF COMPANIES  
 Australia - Brazil - Canada - China - Finland - France - Germany  
 Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore  
 Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>

