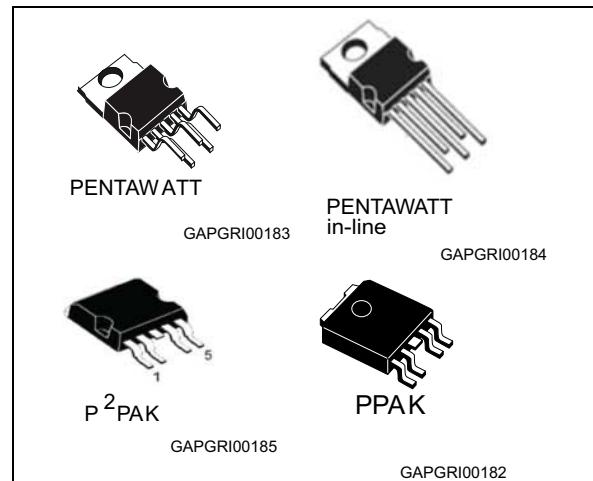


Features

| Type | $R_{DS(on)}$ | I_{OUT} | V_{CC} |
|---|---------------|-----------|----------|
| VN750-E VN750PT-E VN750B5-E VN750-12-E | 60 m Ω | 6 A | 36 V |

- ECOPACK[®]: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection



Description

The VN750-E is a monolithic device designed in STMicroelectronics[®] VIPower[®] M0-3 technology intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart help protect the device against overload.

The device detects open load condition in on-state and off-state. Output shorted to V_{CC} is detected in the off-state. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

| Package | Order codes | |
|--------------------|-------------|---------------|
| | Tube | Tape and reel |
| PENTAWATT | VN750-E | - |
| P ² PAK | VN750B5-E | VN750B5TR-E |
| PPAK | VN750PT-E | VN750PTTR-E |
| PENTAWATT in-line | VN750-12-E | - |

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1 Block diagram and pin description

Figure 1. Block diagram

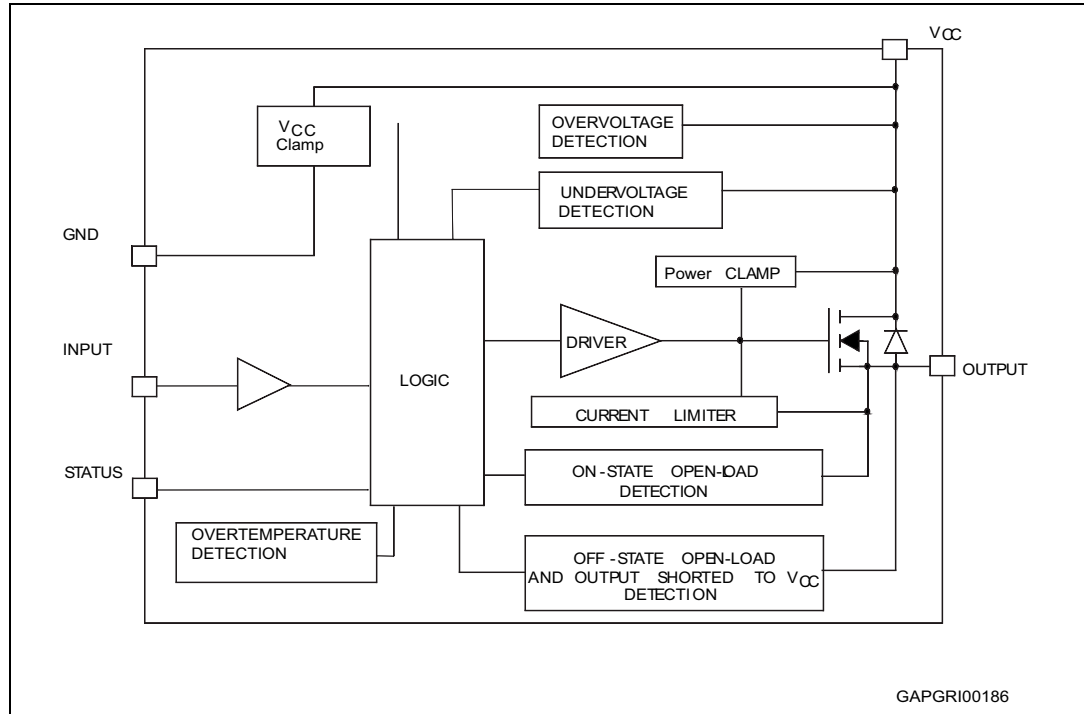


Figure 2. Configuration diagram (top view)

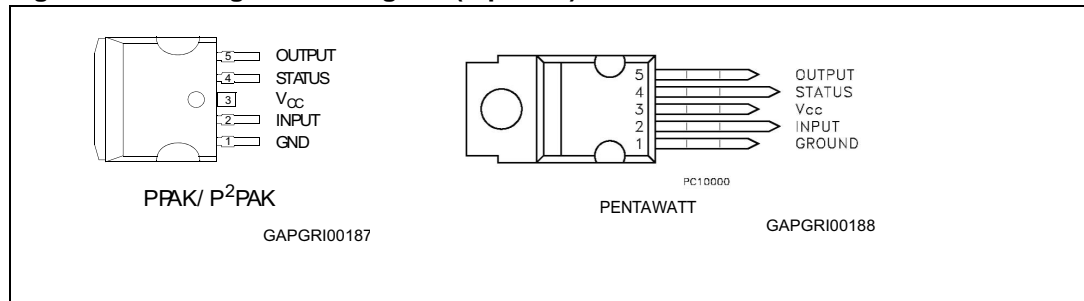
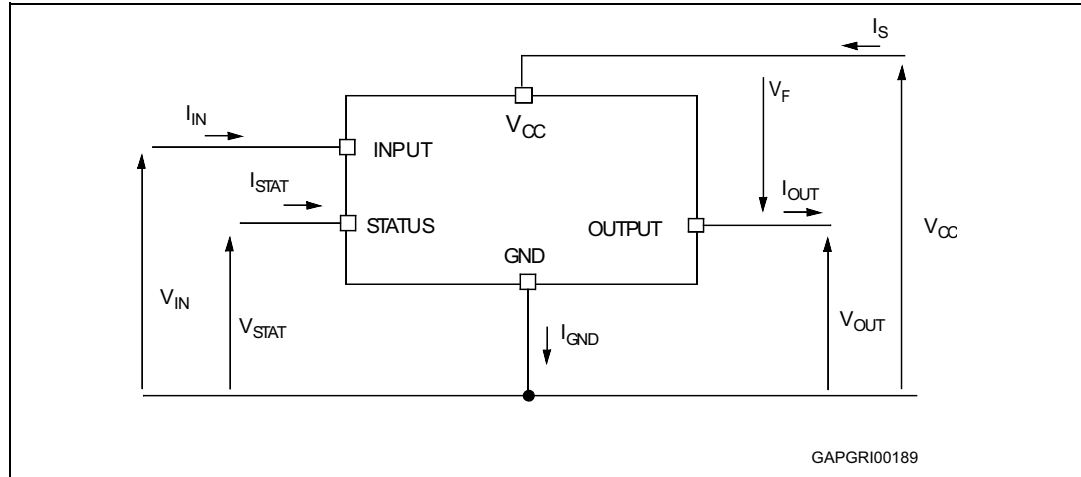


Table 2. Suggested connections for unused and not connected pins

| Connection/pin | Status | N.C. | Output | Input |
|----------------|--------|------|--------|------------------------|
| Floating | X | X | X | X |
| To ground | | X | | Through 10 KΩ resistor |

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stress values that exceed those listed in the “Absolute maximum ratings” table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | | | Unit |
|------------|---|--------------------|--------------------|------|------|
| | | PENTAWATT | P ² PAK | PPAK | |
| V_{CC} | DC supply voltage | 41 | | | V |
| $-V_{CC}$ | Reverse DC supply voltage | - 0.3 | | | V |
| $-I_{gnd}$ | DC reverse ground pin current | - 200 | | | mA |
| I_{OUT} | DC output current | Internally limited | | | A |
| $-I_{OUT}$ | Reverse DC output current | - 6 | | | A |
| I_{IN} | DC input current | +/- 10 | | | mA |
| I_{STAT} | DC status current | +/- 10 | | | mA |
| V_{ESD} | Electrostatic discharge (human body model: R=1.5 KΩ; C=100pF) | | | | |
| | - Input | 4000 | | | V |
| | - Status | 4000 | | | V |
| | - Output | 5000 | | | V |
| | - V_{CC} | 5000 | | | V |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | | | Unit |
|------------------|---|--------------------|--------------------|------|------|
| | | PENTAWATT | P ² PAK | PPAK | |
| E _{MAX} | Maximum switching energy (L=2.46 mH; R _L =0 Ω; V _{bat} =13.5 V; T _{jstart} =150 °C; I _L =9 A) | | 138 | 138 | mJ |
| P _{tot} | Power dissipation T _C =25°C | 60 | | | W |
| T _j | Junction operating temperature | Internally limited | | | °C |
| T _C | Case operating temperature | - 40 to 150 | | | °C |
| T _{stg} | Storage temperature | - 55 to 150 | | | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Max. value | | | Unit |
|-----------------------|-------------------------------------|------------|---------------------|---------------------|------|
| | | PENTAWATT | P ² PAK | PPAK | |
| R _{thj-case} | Thermal resistance junction-case | 2.1 | 2.1 | 2.1 | °C/W |
| R _{thj-lead} | Thermal resistance junction-lead | - | - | - | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient | 62.1 | 52.1 ⁽¹⁾ | 77.1 ⁽¹⁾ | °C/W |
| | | 62.1 | 37 ⁽²⁾ | 44 ⁽²⁾ | °C/W |

1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C, unless otherwise stated.

Table 5. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|----------------------------------|---|------|------|------|------|
| Power | | | | | | |
| V _{CC} | Operating supply voltage | | 5.5 | 13 | 36 | V |
| V _{USD} | Undervoltage shutdown | | 3 | 4 | 5.5 | V |
| V _{USDhyst} | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| V _{OV} | Overvoltage shutdown | | 36 | | | V |
| R _{ON} | On-state resistance | I _{OUT} =2 A; T _j =25 °C; V _{CC} > 8 V | | | 60 | mΩ |
| | | I _{OUT} =2 A; V _{CC} > 8 V | | | 120 | mΩ |

Table 5. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|------------------------------|---|--------------------------------|------|------|------------------------|
| I_S | Supply current | Off-state; $V_{CC}=13\text{ V}$; $V_{IN}=V_{OUT}=0\text{ V}$ | | 10 | 25 | μA |
| | | Off-state; $V_{CC}=13\text{ V}$; $V_{IN}=V_{OUT}=0\text{ V}$; $T_j=25\text{ }^\circ\text{C}$ | | 10 | 20 | μA |
| | | On-state; $V_{CC}=13\text{ V}$; $V_{IN}=5\text{ V}$; $I_{OUT}=0\text{ A}$ | | 2 | 3.5 | mA |
| $I_{L(off1)}$ | Off-state output current | $V_{IN}=V_{OUT}=0\text{ V}$ | 0 | | 50 | μA |
| $I_{L(off2)}$ | Off-state output current | $V_{IN}=0\text{ V}$; $V_{OUT}=3.5\text{ V}$ | -75 | | 0 | μA |
| $I_{L(off3)}$ | Off-state output current | $V_{IN}=V_{OUT}=0\text{ V}$; $V_{CC}=13\text{ V}$; $T_j=125\text{ }^\circ\text{C}$ | | | 5 | μA |
| $I_{L(off4)}$ | Off-state output current | $V_{IN}=V_{OUT}=0\text{ V}$; $V_{CC}=13\text{ V}$; $T_j=25\text{ }^\circ\text{C}$ | | | 3 | μA |
| Switching ($V_{CC}=13\text{ V}$) | | | | | | |
| $t_{d(on)}$ | Turn-on delay time | $R_L=6.5\ \Omega$ from V_{IN} rising edge to $V_{OUT}=1.3\text{ V}$ | | 40 | | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L=6.5\ \Omega$ from V_{IN} falling edge to $V_{OUT}=11.7\text{ V}$ | | 30 | | μs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L=6.5\ \Omega$ from $V_{OUT}=1.3\text{ V}$ to $V_{OUT}=10.4\text{ V}$ | See Figure 21. | | | $\text{V}/\mu\text{s}$ |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L=6.5\ \Omega$ from $V_{OUT}=11.7\text{ V}$ to $V_{OUT}=1.3\text{ V}$ | See Figure 22. | | | $\text{V}/\mu\text{s}$ |
| Input pin | | | | | | |
| V_{IL} | Input low level | | | | 1.25 | V |
| I_{IL} | Low level input current | $V_{IN}=1.25\text{ V}$ | 1 | | | μA |
| V_{IH} | Input high level | | 3.25 | | | V |
| I_{IH} | High level input current | $V_{IN}=3.25\text{ V}$ | | | 10 | μA |
| V_{hyst} | Input hysteresis voltage | | 0.5 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN}=1\text{ mA}$ $I_{IN}=-1\text{ mA}$ | 6 | 6.8 | 8 | V |
| | | | | -0.7 | | V |
| V_{CC} output diode | | | | | | |
| V_F | Forward on voltage | $-I_{OUT}=1.3\text{ A}$; $T_j=150\text{ }^\circ\text{C}$ | | | 0.6 | V |
| Status pin | | | | | | |
| V_{STAT} | Status low output voltage | $I_{STAT}=1.6\text{ mA}$ | | | 0.5 | V |
| I_{LSTAT} | Status leakage current | Normal operation; $V_{STAT}=5\text{ V}$ | | | 10 | μA |
| C_{STAT} | Status pin input capacitance | Normal operation; $V_{STAT}=5\text{ V}$ | | | 100 | pF |
| V_{SCL} | Status clamp voltage | $I_{STAT}=1\text{ mA}$ $I_{STAT}=-1\text{ mA}$ | 6 | 6.8 | 8 | V |
| | | | | -0.7 | | V |
| Protections⁽¹⁾ | | | | | | |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^\circ\text{C}$ |

Table 5. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|---|--|---------------|---------------|---------------|--------|
| T_R | Reset temperature | | 135 | | | °C |
| T_{hyst} | Thermal hysteresis | | 7 | 15 | | °C |
| t_{SDL} | Status delay in overload condition | $T_j > T_{jsh}$ | | | 20 | ms |
| I_{lim} | Current limitation | $9 V < V_{CC} < 36 V$ $5 V < V_{CC} < 36 V$ | 6 | 9 | 15 15 | A A |
| V_{demag} | Turn-off output clamp voltage | $I_{OUT} = 2 A; V_{IN} = 0 V; L = 6 mH$ | $V_{CC} - 41$ | $V_{CC} - 48$ | $V_{CC} - 55$ | V |
| Open-load detection | | | | | | |
| I_{OL} | Open-load on state detection threshold | $V_{IN} = 5 V$ | 50 | | 200 | mA |
| $t_{DOL(on)}$ | Open-load on state detection delay | $I_{OUT} = 0 A$ | | | 200 | µs |
| V_{OL} | Open-load off state voltage detection threshold | $V_{IN} = 0 V$ | 1.5 | | 3.5 | V |
| $t_{DOL(off)}$ | Open-load detection delay at turn-off | | | | 1000 | µs |

- To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Figure 4. Status timings

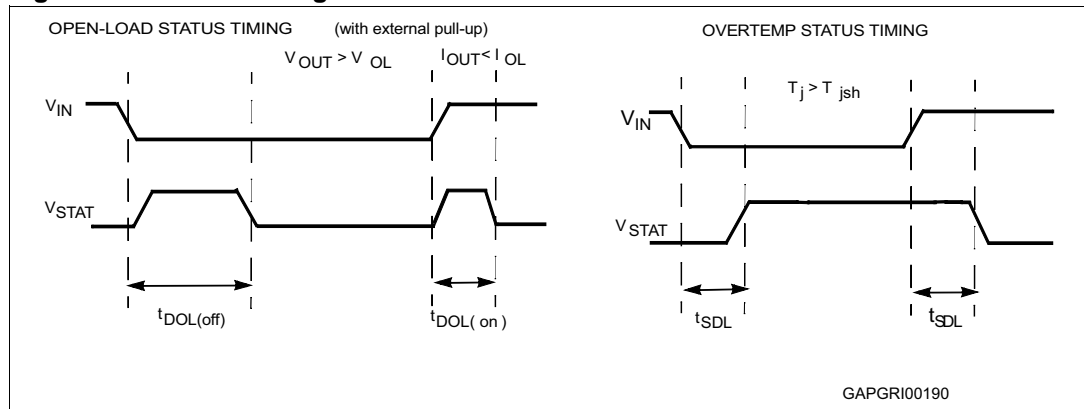


Figure 5. Switching time waveforms

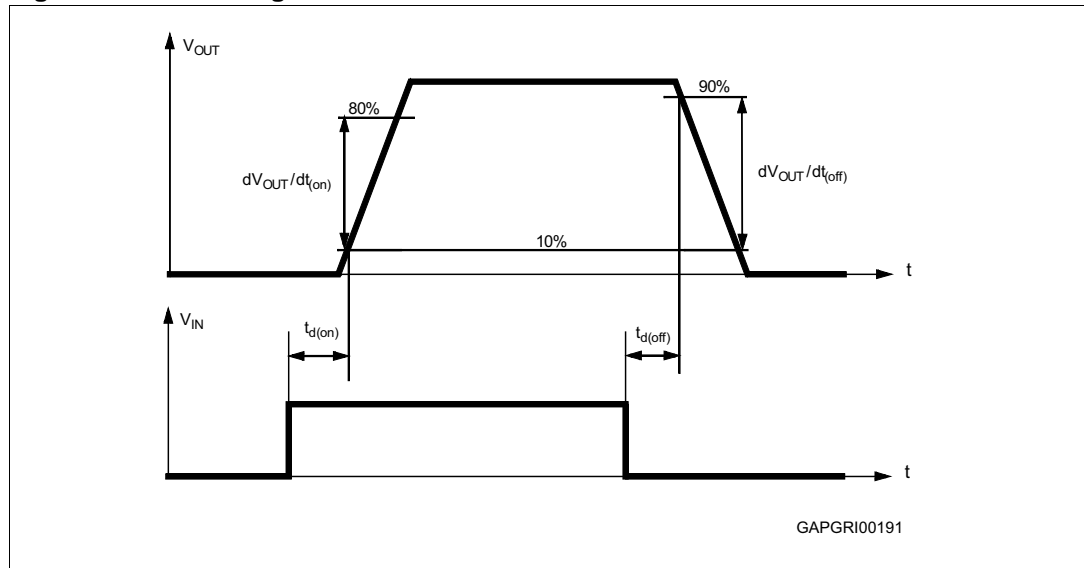


Table 6. Truth table

| Conditions | Input | Output | Status |
|---------------------------|-------|--------|--|
| Normal operation | L | L | H |
| | H | H | H |
| Current limitation | L | L | H |
| | H | X | ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L |
| Over temperature | L | L | H |
| | H | L | L |
| Undervoltage | L | L | X |
| | H | L | X |
| Overvoltage | L | L | H |
| | H | L | H |
| Output voltage > V_{OL} | L | H | L |
| | H | H | H |
| Output current < I_{OL} | L | L | H |
| | H | H | L |

Table 7. Electrical transient requirements on V_{CC} pin (part 1/3)

| ISO T/R 7637/1 test pulse | Test levels | | | | Delays and impedance |
|---------------------------|-------------|-------|--------|--------|-------------------------|
| | I | II | III | IV | |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 μ s 50 Ω |

Table 7. Electrical transient requirements on V_{CC} pin (part 1/3) (continued)

| ISO T/R 7637/1 test pulse | Test levels | | | | Delays and impedance |
|------------------------------|-------------|---------|---------|---------|-------------------------|
| | I | II | III | IV | |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 μs 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |
| 5 | +26.5 V | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 Ω |

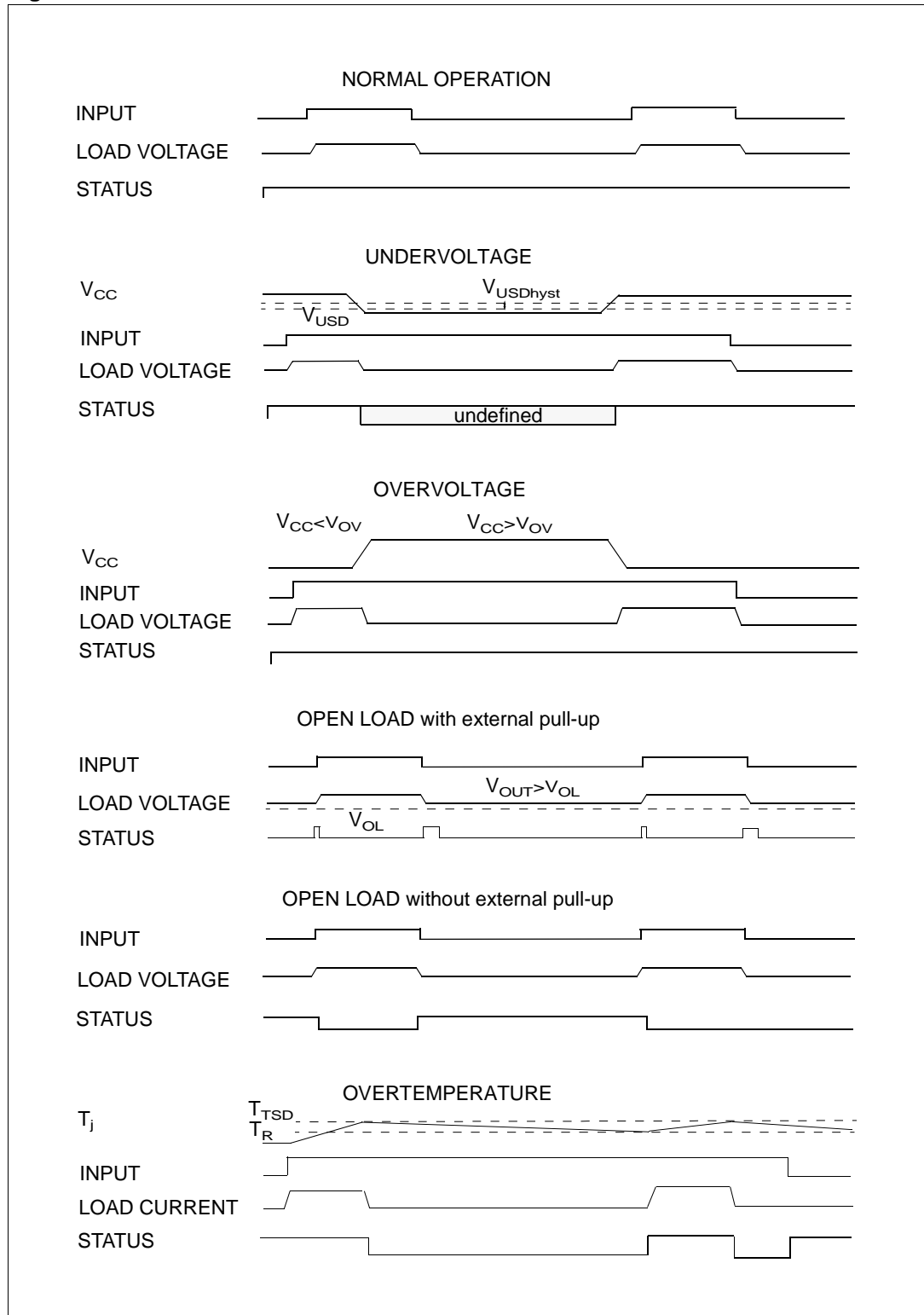
Table 8. Electrical transient requirements on V_{CC} pin (part 2/3)

| ISO T/R 7637/1 test pulse | Test levels results | | | |
|------------------------------|---------------------|----|-----|----|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

Table 9. Electrical transient requirements on V_{CC} pin (part 3/3)

| Class | Contents |
|-------|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

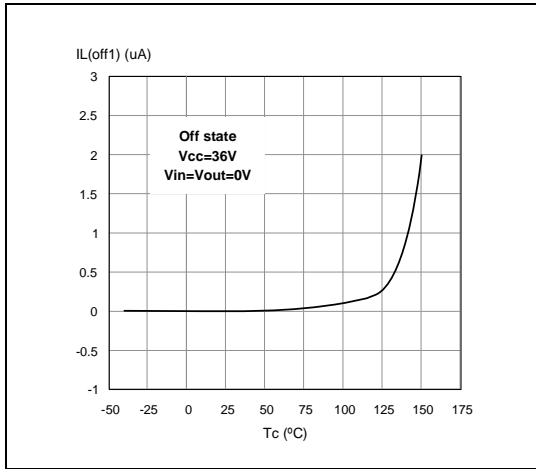


Figure 8. High level input current

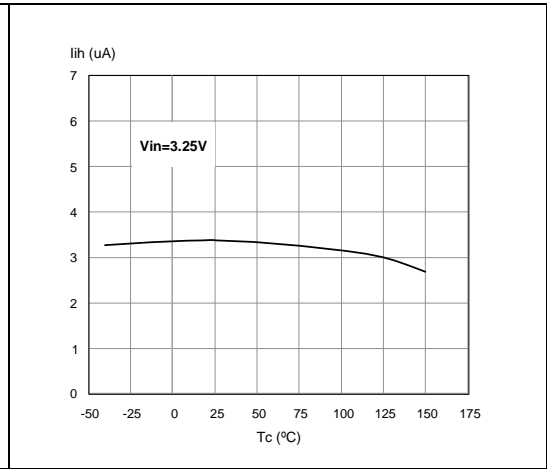


Figure 9. Input clamp voltage

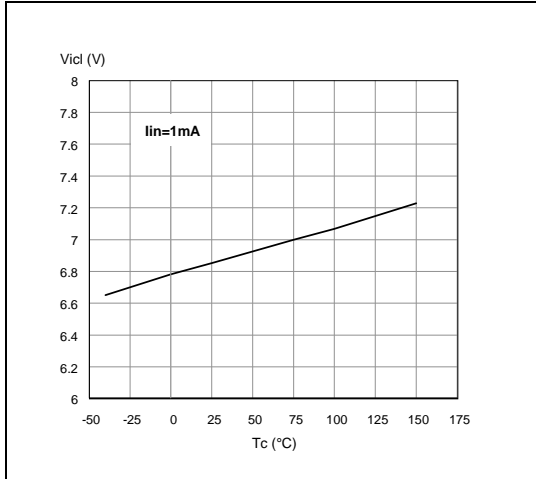


Figure 10. Status leakage current

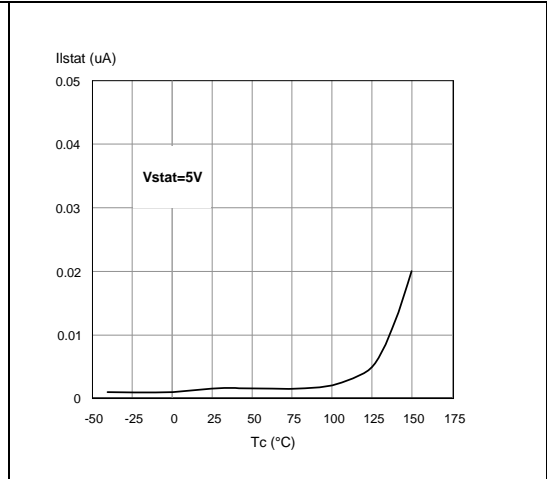


Figure 11. Status low output voltage

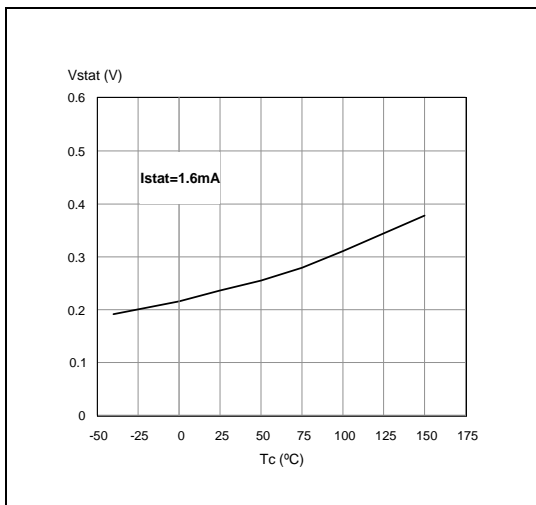


Figure 12. Status clamp voltage

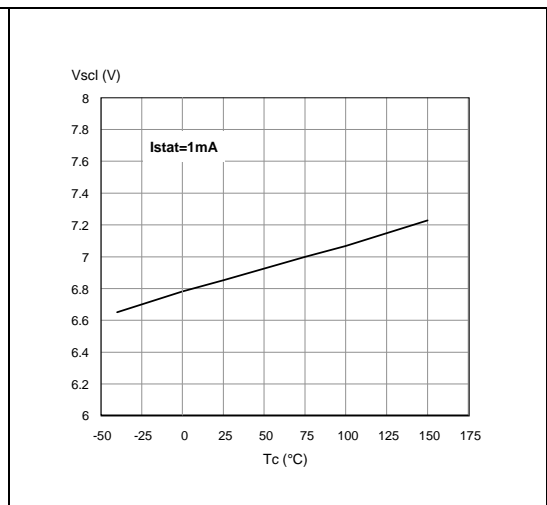


Figure 13. On-state resistance Vs T_{case}

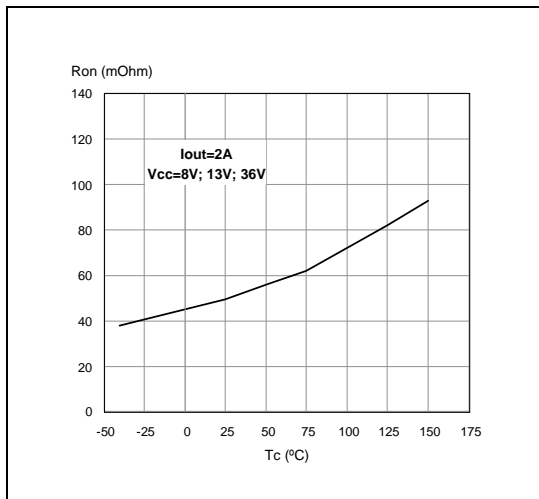


Figure 14. On-state resistance Vs V_{CC}

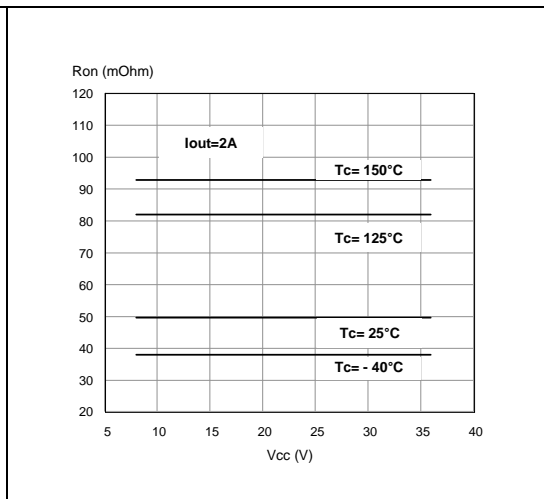


Figure 15. Open-load on-state detection

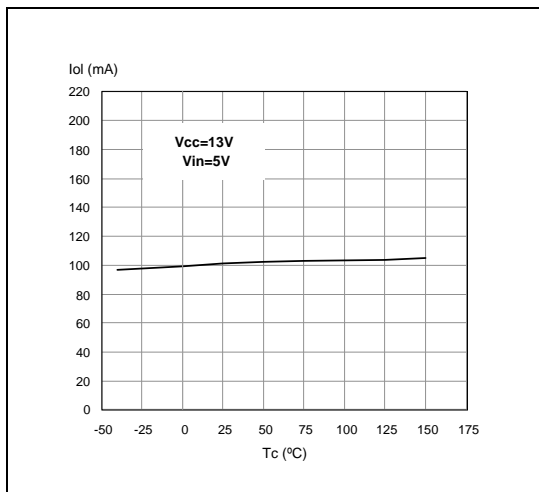


Figure 16. Input high level threshold

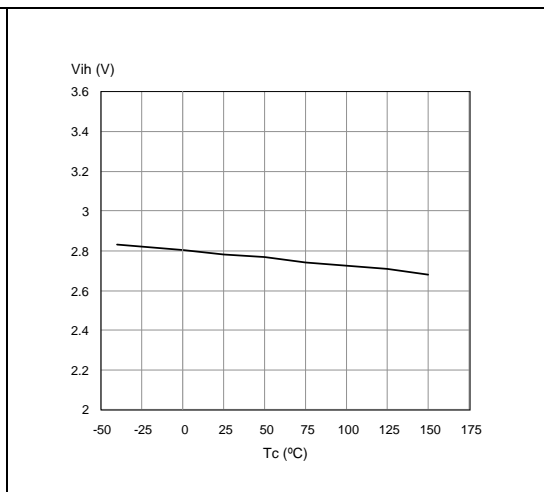


Figure 17. Input low level

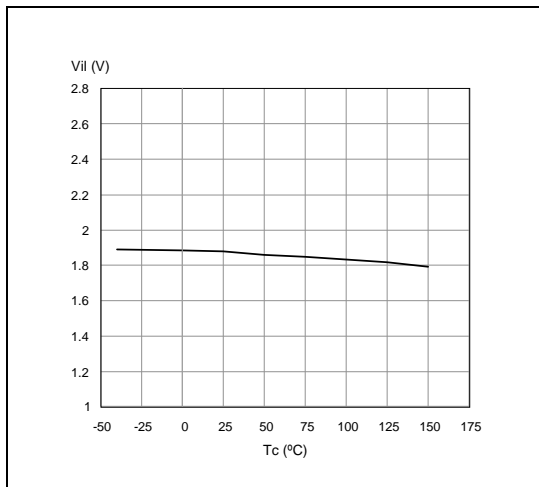


Figure 18. Input hysteresis voltage

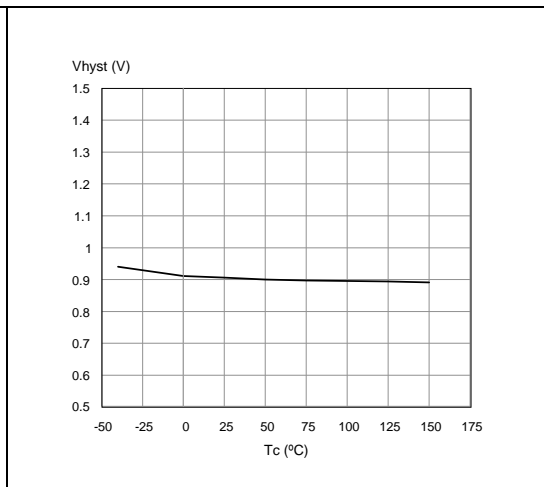


Figure 19. Overtoltage shutdown

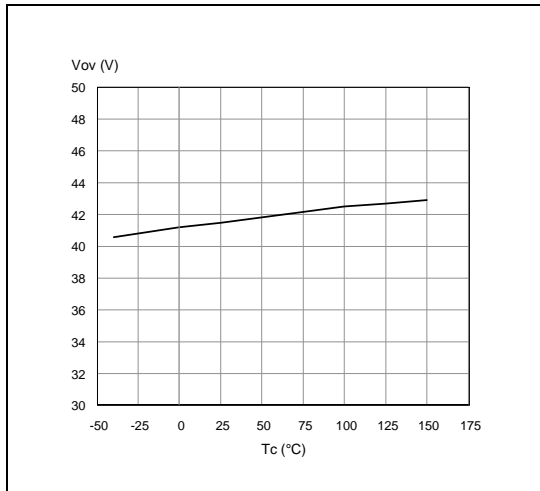


Figure 20. Open-load off-state voltage detection threshold

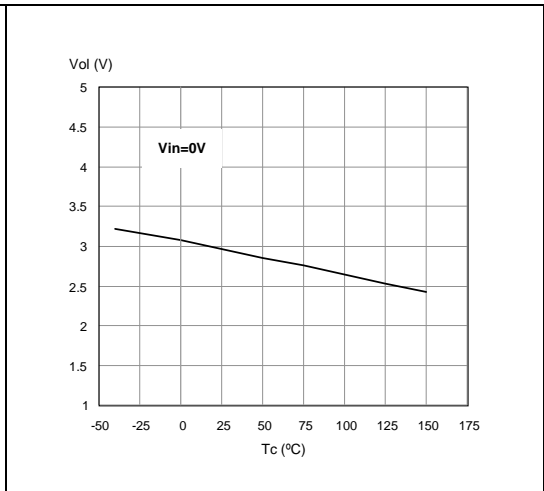


Figure 21. Turn-on voltage slope

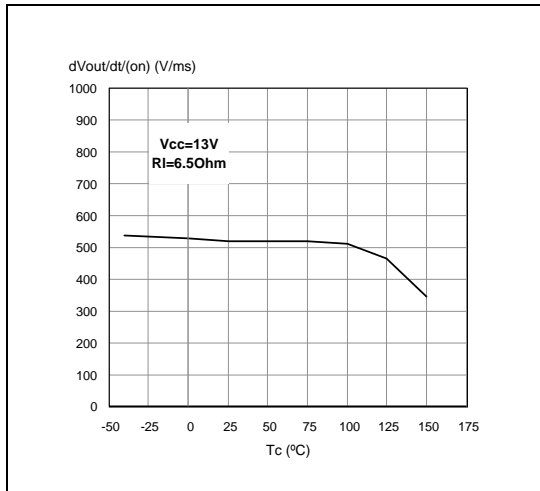


Figure 22. Turn-off voltage slope

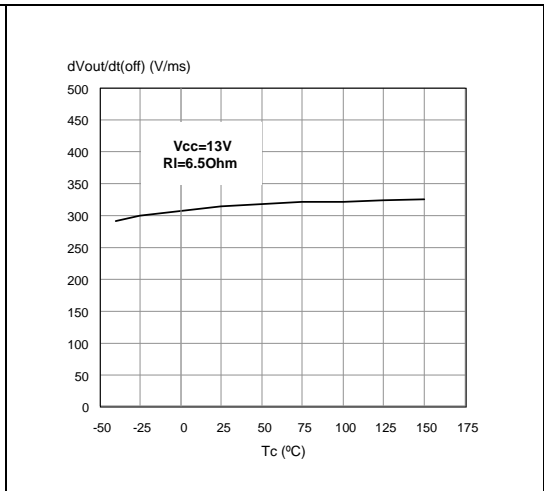


Figure 23. Ilim Vs Tcase

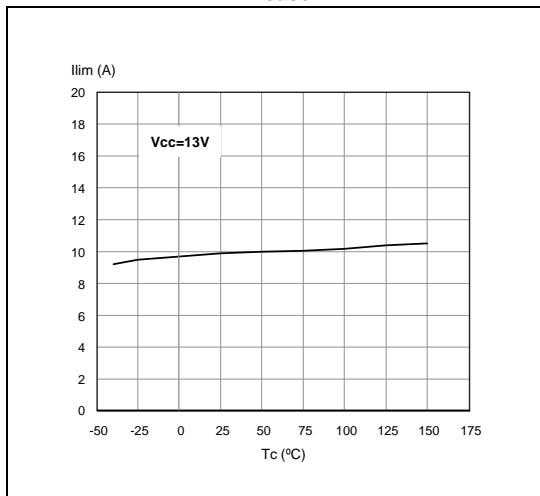
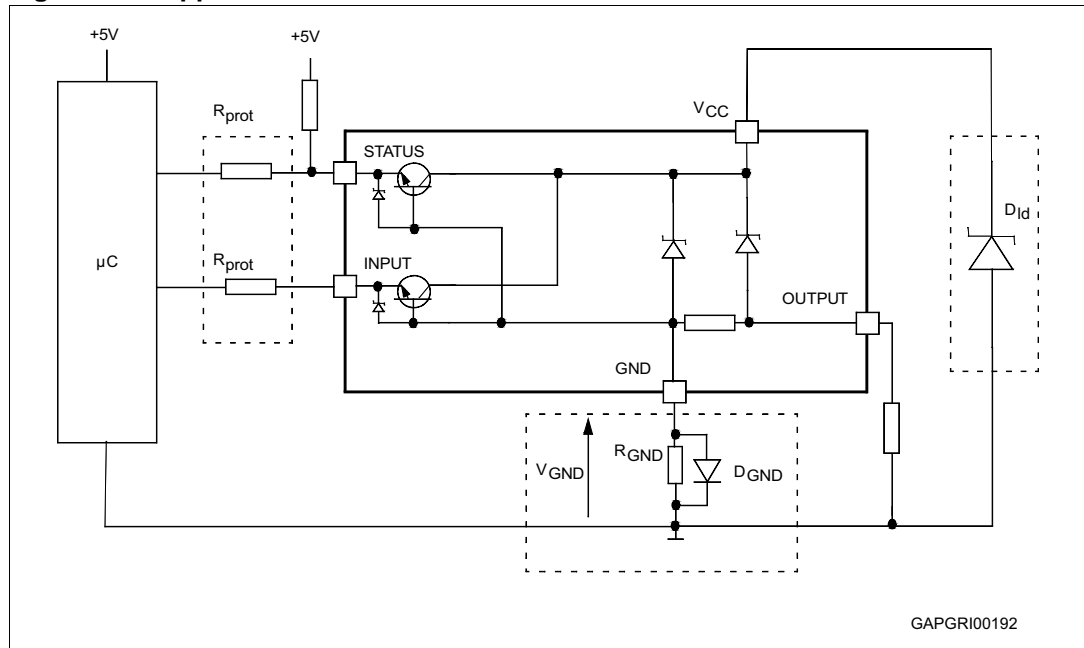


Figure 24. Application schematic



2.5 GND protection network against reverse battery

2.5.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (2.5.2: [Solution 2: diode \(D_{GND}\) in the ground line](#)).

2.5.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1\text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600\text{mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in input and status lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

The safest configuration for unused input and status pin is to leave them unconnected.

2.6 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

2.7 Microcontroller I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with from latching-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{ V}$ and $I_{latchup} \geq 20\text{ mA}$; $V_{OH\mu C} \geq 4.5\text{ V}$

$$5\text{ k}\Omega \leq R_{prot} \leq 65\text{ k}\Omega$$

Recommended values: $R_{prot} = 10\text{ k}\Omega$.

2.8 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between output pin and a positive supply voltage (V_{PU}) like the +5 V line used to supply the microprocessor.

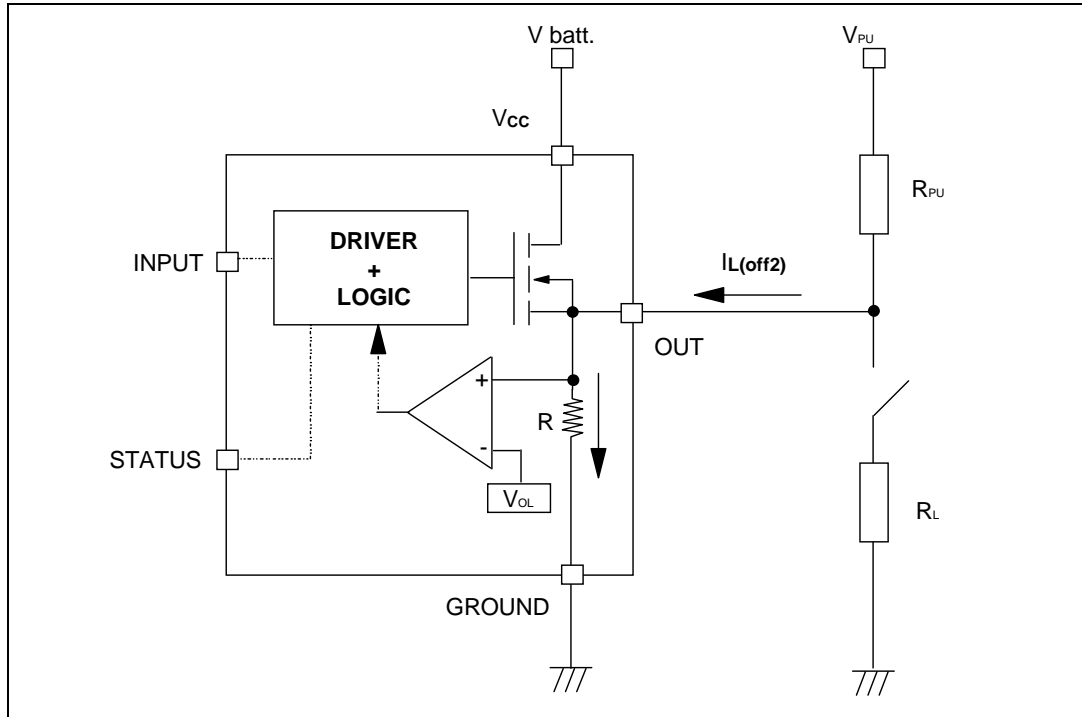
The external resistor has to be selected according to the following requirements:

- no false open-load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$.
- no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched off when the module is in standby.

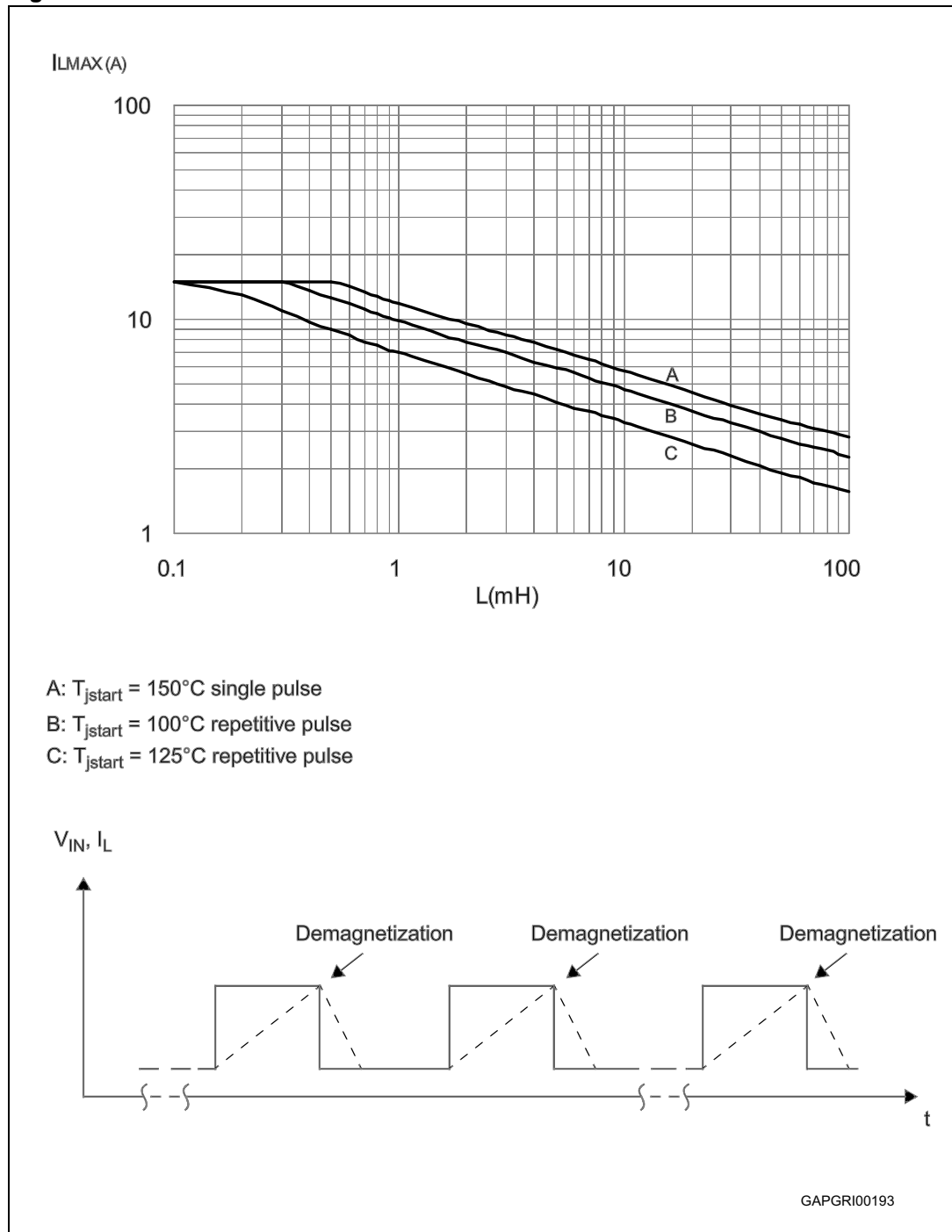
The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open-load detection in off-state



2.9 PPAK/P²PAK maximum demagnetization energy ($V_{CC}=13.5V$)

Figure 26. PPAK /P²PAK maximum turn-off current versus inductance

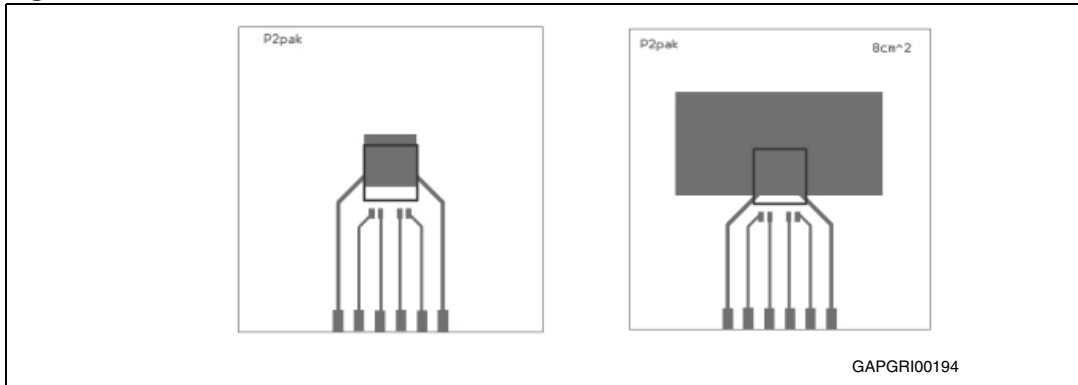


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3 Package and PCB thermal data

3.1 P²PAK thermal data

Figure 27. P²PAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: 0.97 cm², 8 cm²).

Figure 28. P²PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

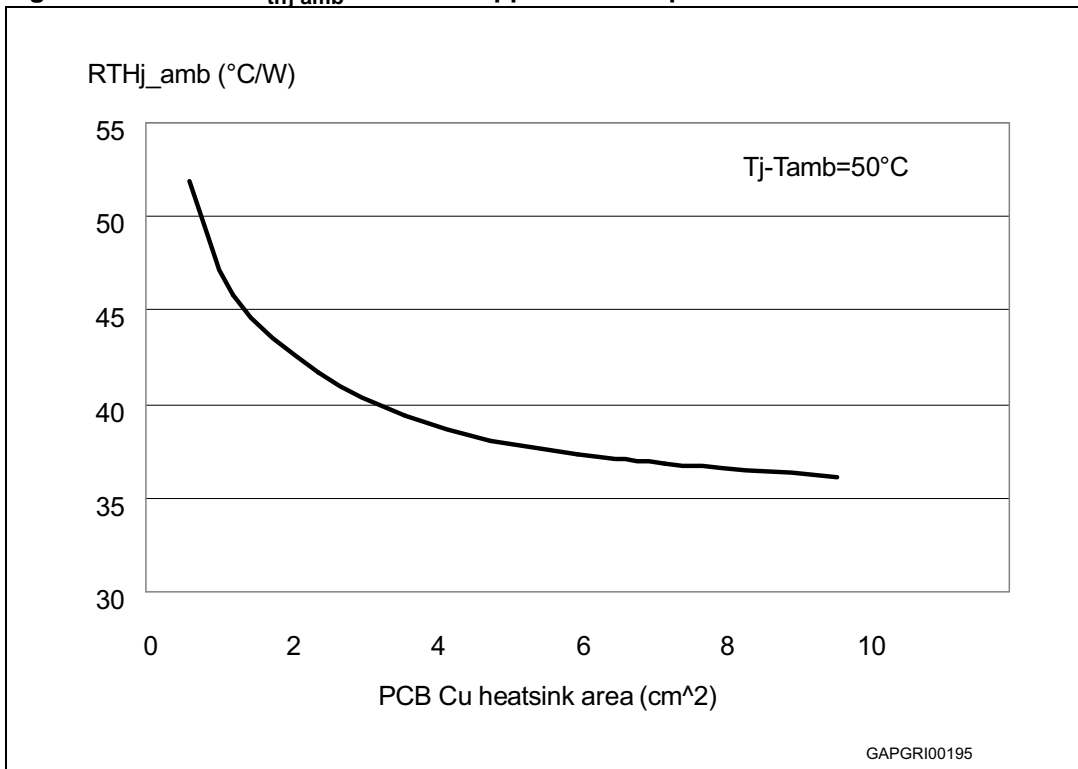
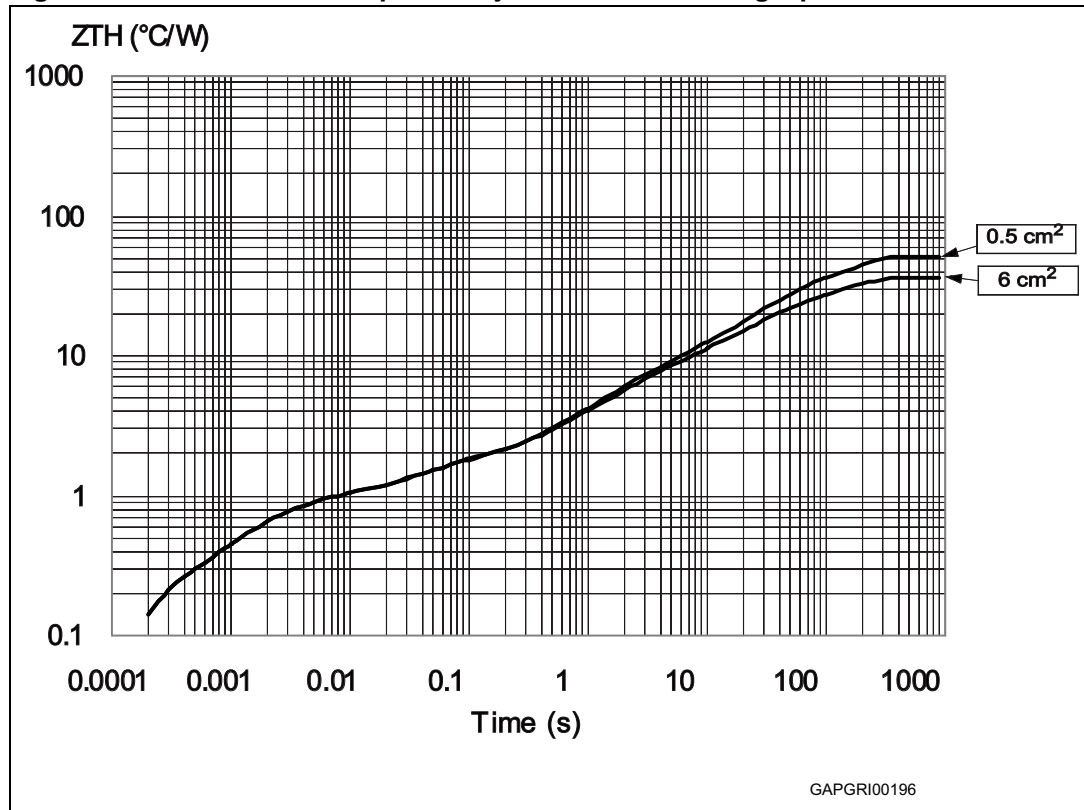


Figure 29. P²PAK thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 30. P²PAK thermal fitting model of a single channel

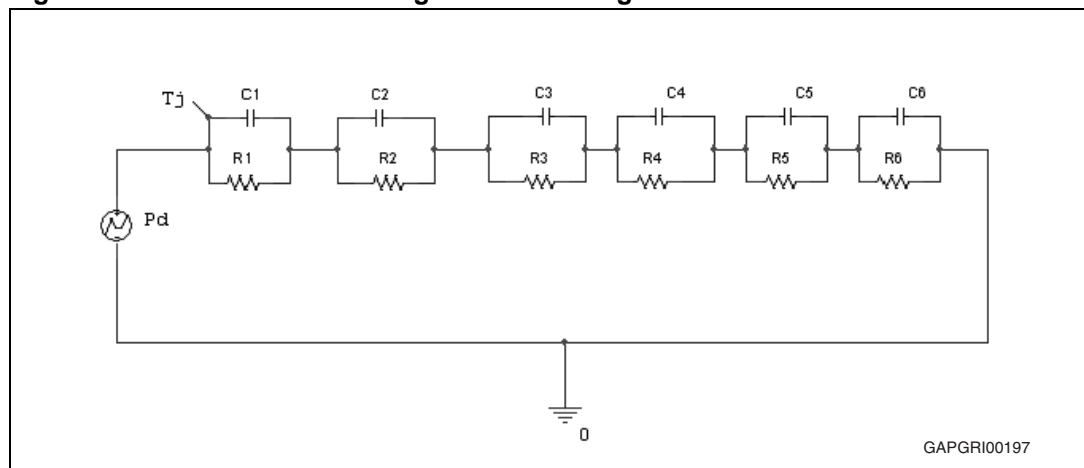
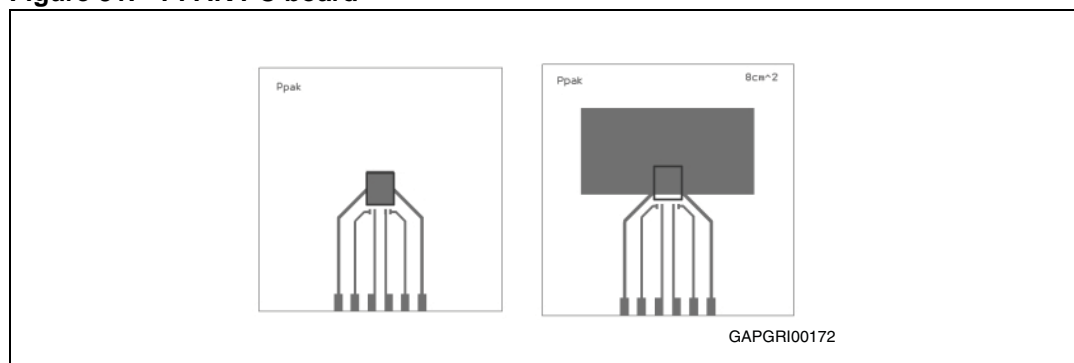


Table 10. P²PAK thermal parameter

| Area/island (cm ²) | 0.5 | 6 |
|--------------------------------|--------|----|
| R1 (°C/W) | 0.15 | |
| R2 (°C/W) | 0.7 | |
| R3 (°C/W) | 0.7 | |
| R4 (°C/W) | 4 | |
| R5 (°C/W) | 9 | |
| R6 (°C/W) | 37 | 22 |
| C1 (W·s/°C) | 0.0006 | |
| C2 (W·s/°C) | 0.0025 | |
| C3 (W·s/°C) | 0.055 | |
| C4 (W·s/°C) | 0.4 | |
| C5 (W·s/°C) | 2 | |
| C6 (W·s/°C) | 3 | 5 |

3.2 PPAK thermal data

Figure 31. PPAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness=35 μ m, Copper areas: 0.44 cm², 8 cm²).

Figure 32. PPAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

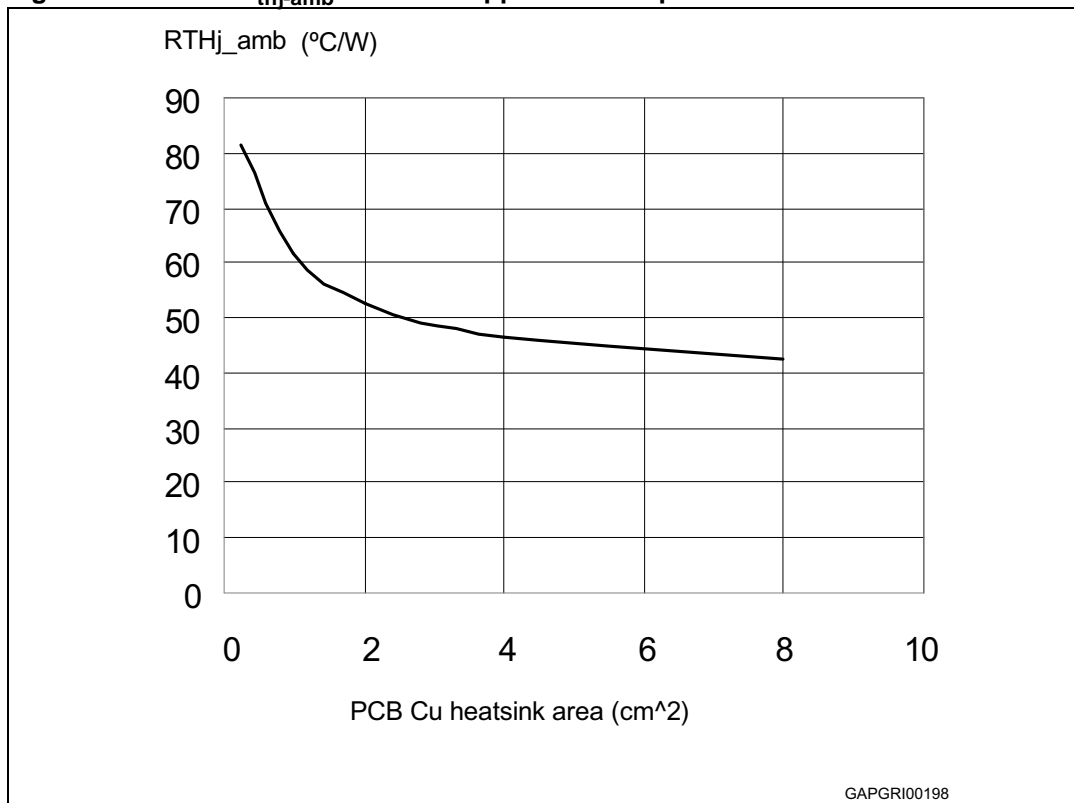
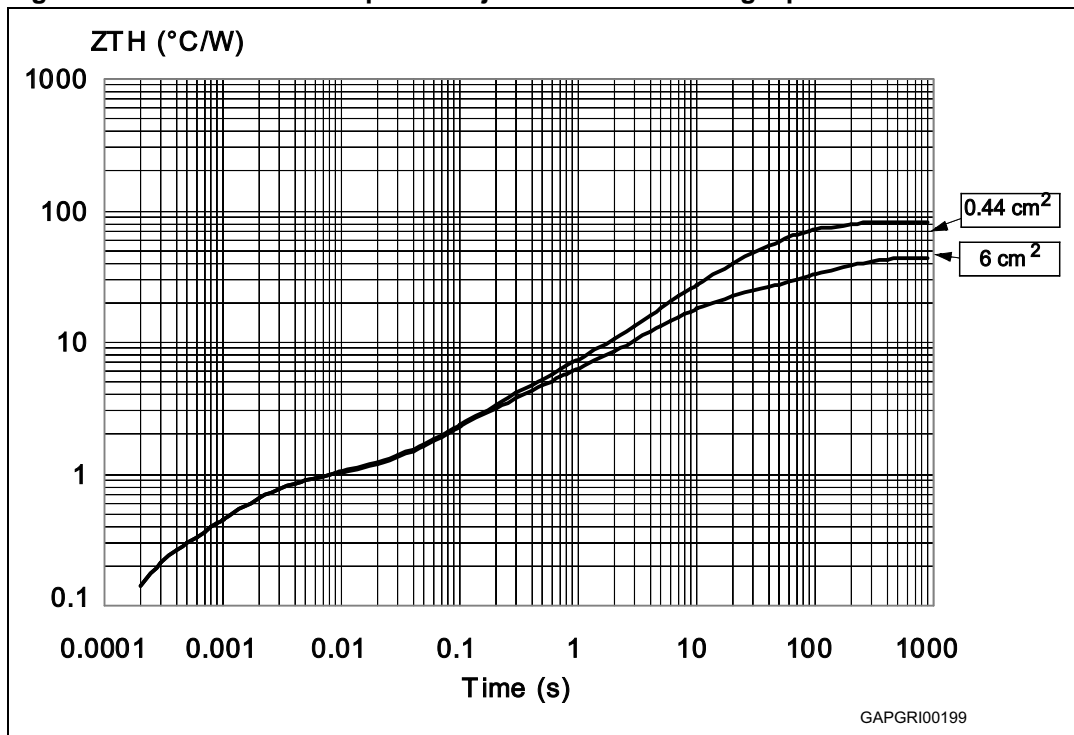


Figure 33. PPAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 34. PPAK thermal fitting model of a single channel

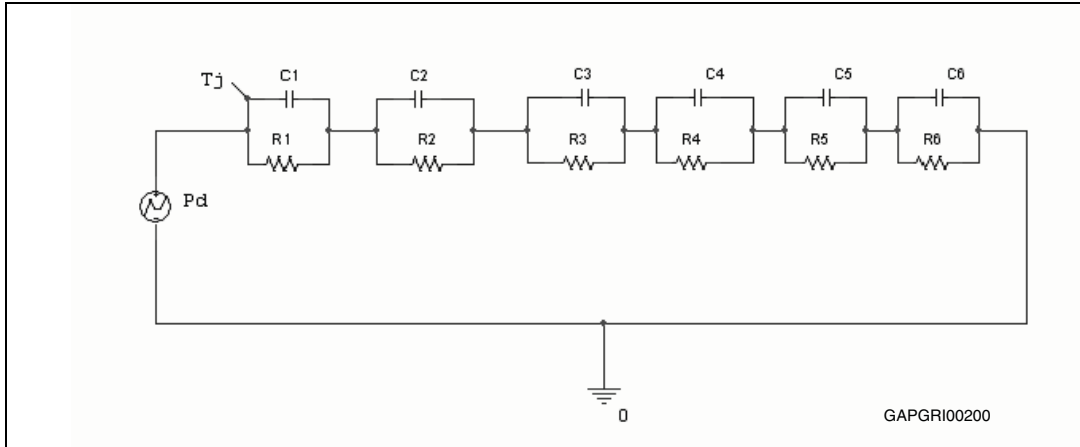


Table 11. PPAK thermal parameter

| Area/island (cm ²) | 0.5 | 6 |
|--------------------------------|--------|----|
| R1 (°C/W) | 0.15 | |
| R2 (°C/W) | 0.7 | |
| R3 (°C/W) | 1.6 | |
| R4 (°C/W) | 2 | |
| R5 (°C/W) | 15 | |
| R6 (°C/W) | 61 | 24 |
| C1 (W·s/°C) | 0.0006 | |
| C2 (W·s/°C) | 0.0025 | |
| C3 (W·s/°C) | 0.08 | |
| C4 (W·s/°C) | 0.3 | |
| C5 (W·s/°C) | 0.45 | |
| C6 (W·s/°C) | 0.8 | 5 |

Table 12. PENTAWATT mechanical data (continued)

| Dim. | mm | | |
|-------|-------|-------|------|
| | Min. | Typ. | Max. |
| D1 | 1.2 | | 1.35 |
| E | 0.35 | | 0.55 |
| F | 0.8 | | 1.05 |
| F1 | 1 | | 1.4 |
| G | 3.2 | 3.4 | 3.6 |
| G1 | 6.6 | 6.8 | 7 |
| H2 | | | 10.4 |
| H3 | 10.05 | | 10.4 |
| L | | 17.85 | |
| L1 | | 15.75 | |
| L2 | | 21.4 | |
| L3 | | 22.5 | |
| L5 | 2.6 | | 3 |
| L6 | 15.1 | | 15.8 |
| L7 | 6 | | 6.6 |
| M | | 4.5 | |
| M1 | | 4 | |
| Diam. | 3.65 | | 3.85 |

4.2.1 PENTAWATT (in-line) mechanical data

Figure 36. PENTAWATT (in-line) package dimensions

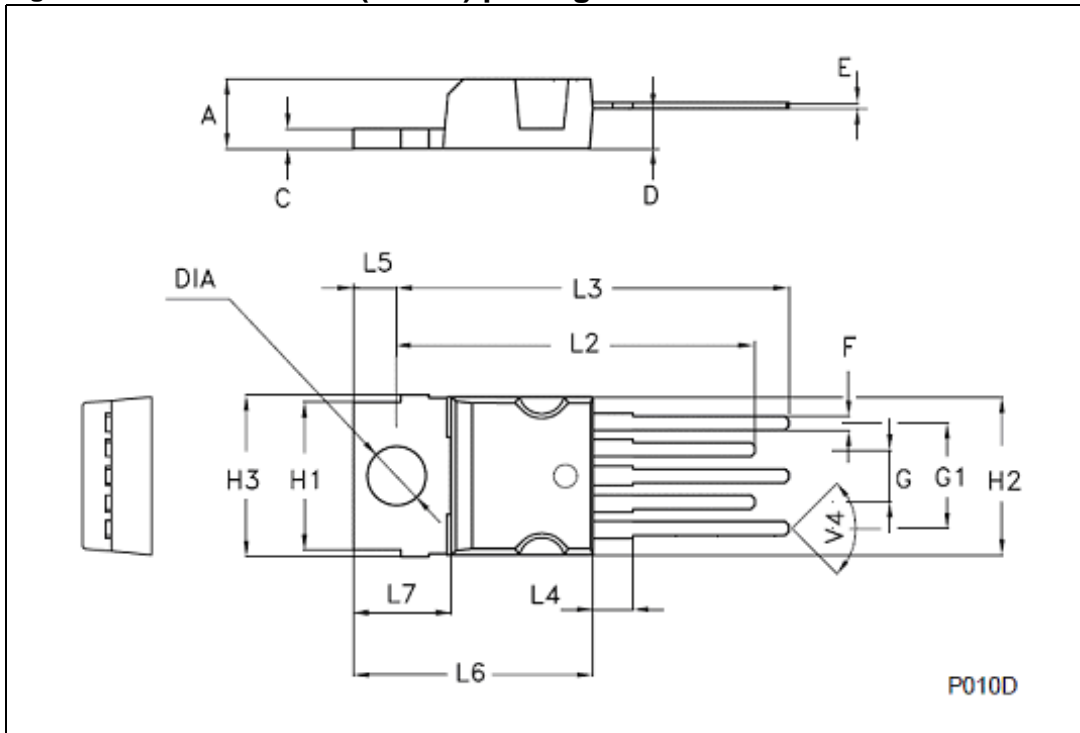


Table 13. PENTAWATT (in-line) mechanical data

| Symbol | millimeters | | |
|--------|-------------|-----|------|
| | Min | Typ | Max |
| A | 4.3 | | 4.8 |
| C | 1.17 | | 1.37 |
| D | 2.4 | | 2.8 |
| E | 0.35 | | 0.55 |
| F | 0.8 | | 1.05 |
| F2 | 1.1 | | 1.4 |
| F3 | 1.25 | | 1.55 |
| G | 3.2 | | 3.6 |
| G1 | 6.6 | | 7 |
| H1 | 9.3 | | 9.7 |
| H2 | | | 10.4 |
| H3 | 10.05 | | 10.4 |
| L2 | 23.05 | | 23.8 |
| L3 | 25.3 | | 26.1 |

Table 13. PENTAWATT (in-line) mechanical data (continued)

| Symbol | millimeters | | |
|--------|-------------|-----|------|
| | Min | Typ | Max |
| L4 | 0.9 | | 2.9 |
| L5 | 2.6 | | 3 |
| L6 | 15.1 | | 15.8 |
| L7 | 6 | | 6.6 |
| V4 | | 90° | |
| Diam. | 3.65 | | 3.85 |

4.3 P²PAK mechanical data

Figure 37. P²PAK package dimensions

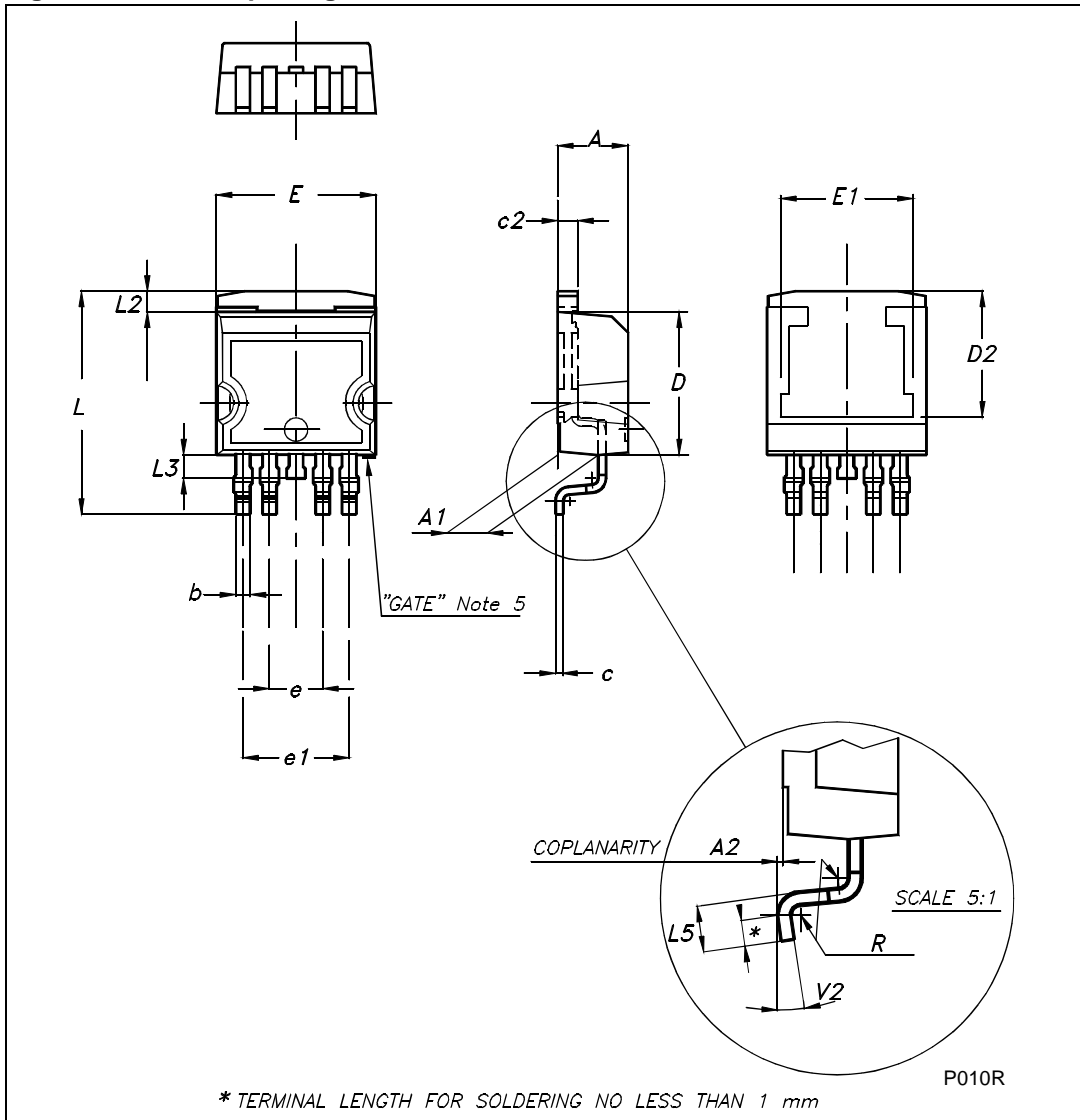


Table 14. P²PAK mechanical data

| Dim. | mm | | |
|----------------|----------------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.30 | | 4.80 |
| A1 | 2.40 | | 2.80 |
| A2 | 0.03 | | 0.23 |
| b | 0.80 | | 1.05 |
| c | 0.45 | | 0.60 |
| c2 | 1.17 | | 1.37 |
| D | 8.95 | | 9.35 |
| D2 | | 8.00 | |
| E | 10.00 | | 10.40 |
| E1 | | 8.50 | |
| e | 3.20 | | 3.60 |
| e1 | 6.60 | | 7.00 |
| L | 13.70 | | 14.50 |
| L2 | 1.25 | | 1.40 |
| L3 | 0.90 | | 1.70 |
| L5 | 1.55 | | 2.40 |
| R | | 0.40 | |
| V2 | 0° | | 8° |
| Package weight | 1.40 Gr. (typ) | | |

4.4 PPAK mechanical data

Figure 38. PPAK package dimensions

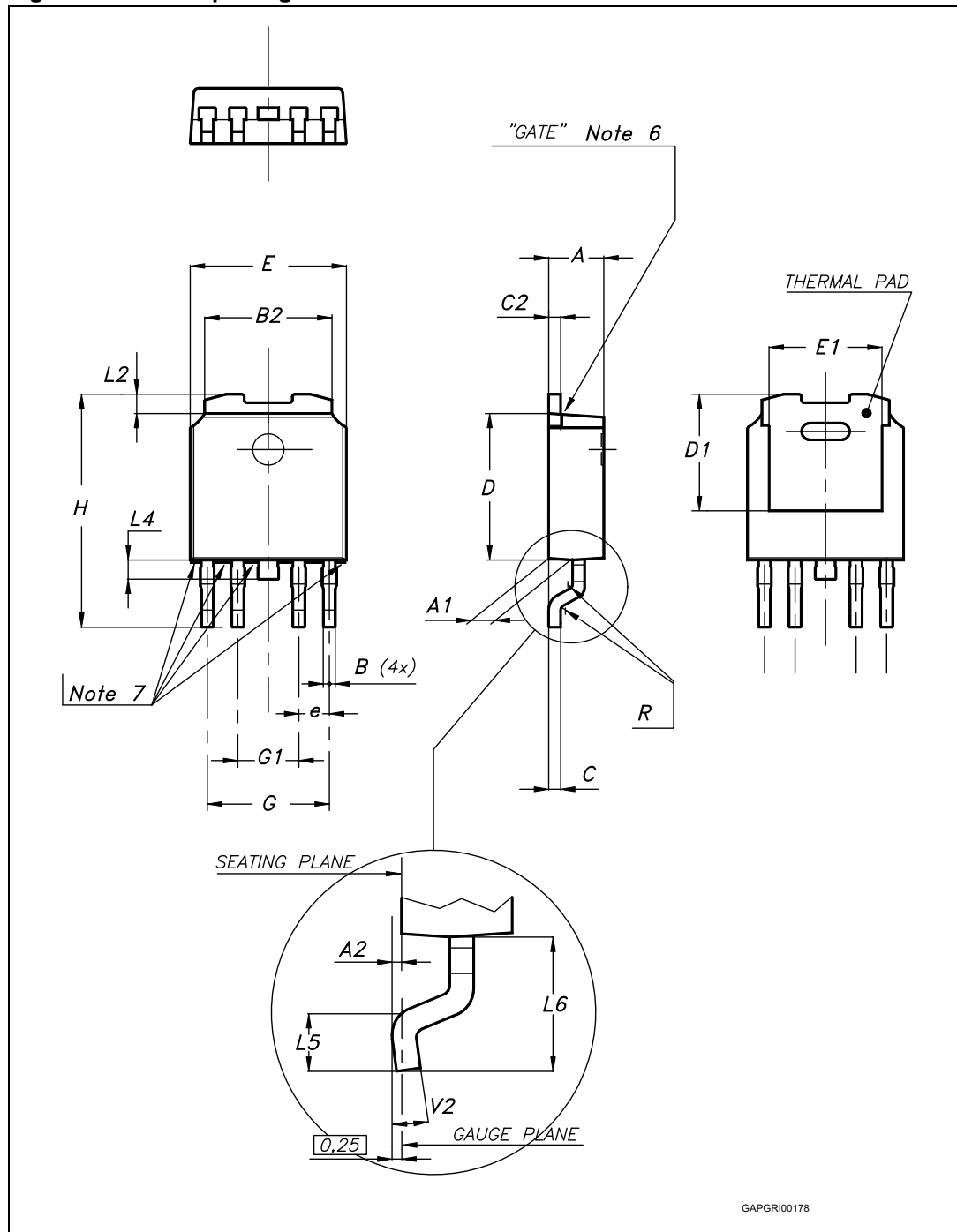


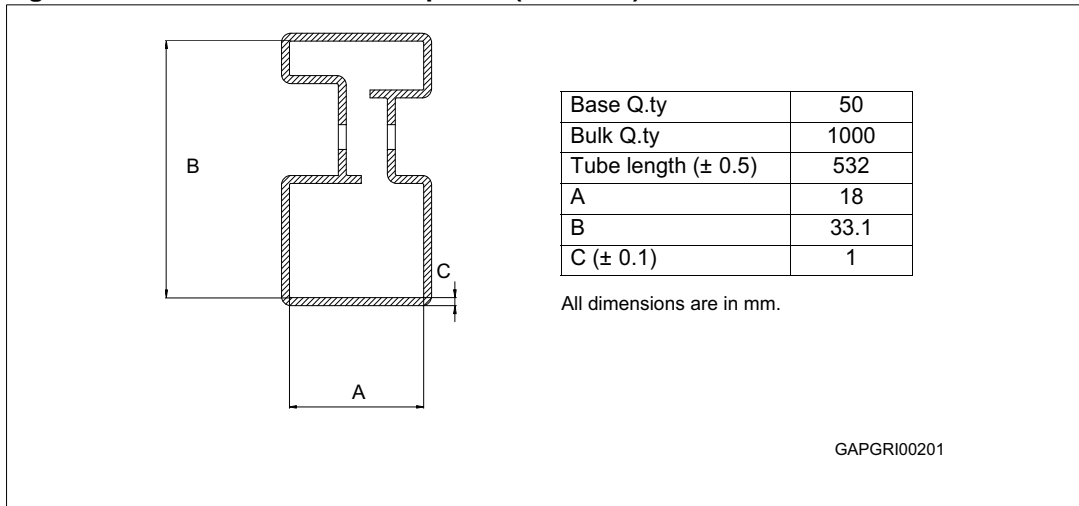
Table 15. PPAK mechanical data

| Dim. | mm | | |
|----------------|---------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| B | 0.40 | | 0.60 |
| B2 | 5.20 | | 5.40 |
| C | 0.45 | | 0.60 |
| C2 | 0.48 | | 0.60 |
| D1 | | 5.1 | |
| D | 6.00 | | 6.20 |
| E | 6.40 | | 6.60 |
| E1 | | 4.7 | |
| e | | 1.27 | |
| G | 4.90 | | 5.25 |
| G1 | 2.38 | | 2.70 |
| H | 9.35 | | 10.10 |
| L2 | | 0.8 | 1.00 |
| L4 | 0.60 | | 1.00 |
| L5 | 1 | | |
| L6 | | 2.80 | |
| R | | 0.2 | |
| V2 | 0° | | 8° |
| Package weight | Gr. 0.3 | | |

4.5 PENTAWATT packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 39. PENTAWATT tube shipment (no suffix)



4.6 P²PAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 40. P²PAK tube shipment (no suffix)

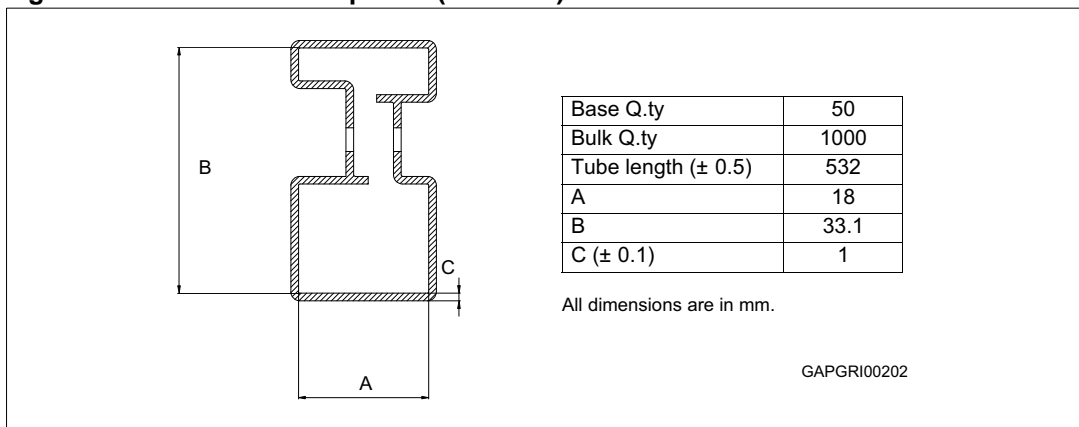
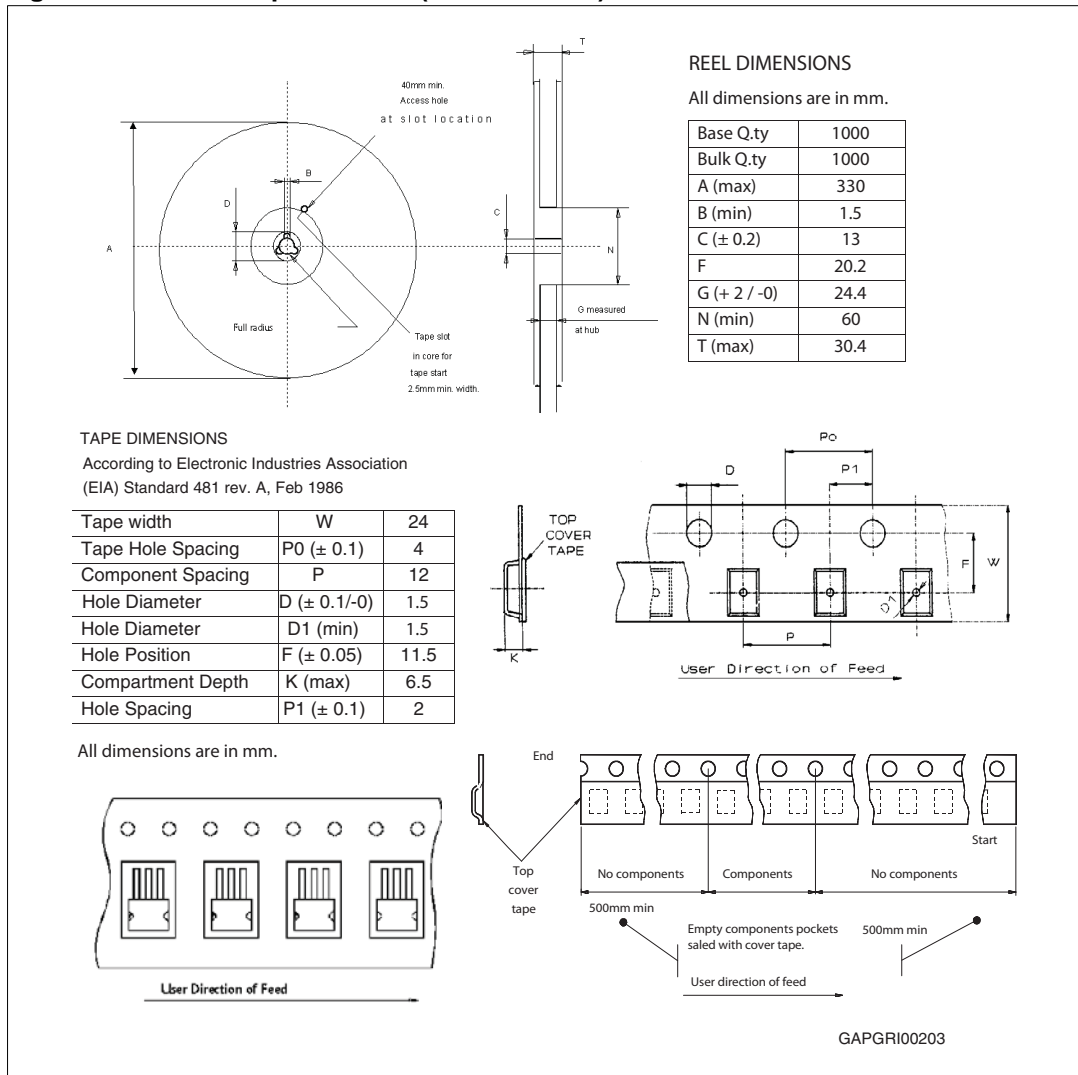


Figure 41. P²PAK tape and reel (suffix “13TR”)



4.7 PPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 42. PPAK suggested pad layout

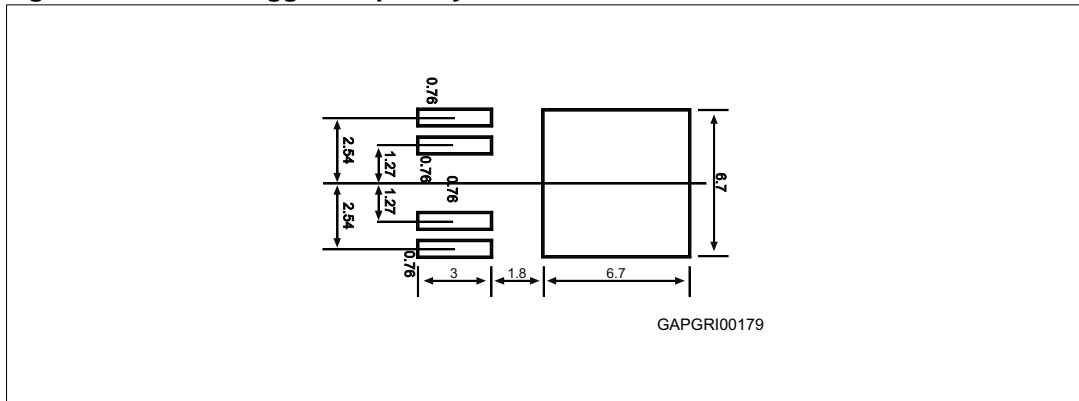
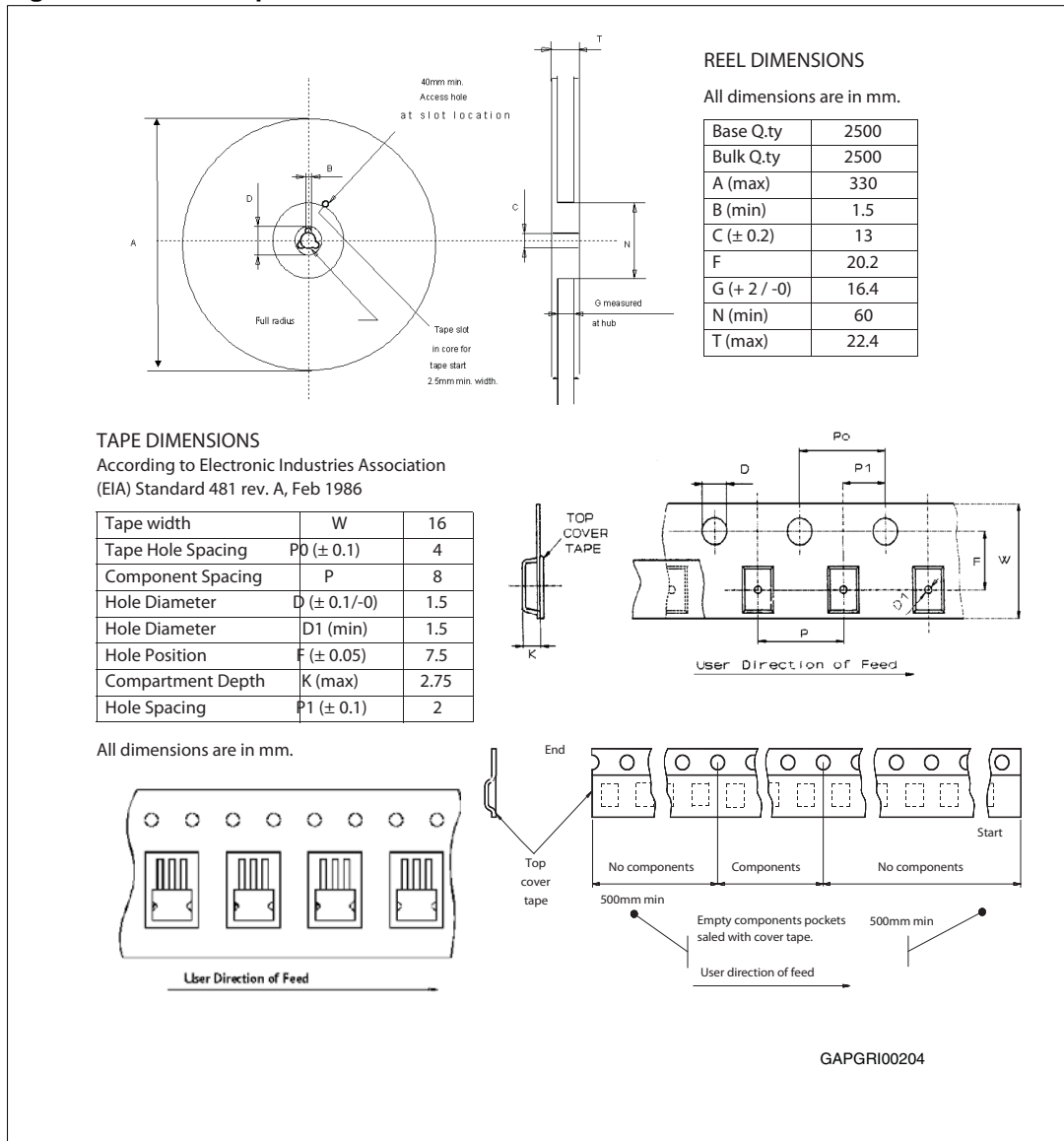


Figure 43. PPAK tube shipment (no suffix)

| | |
|---------------------------|------|
| Base Q.ty | 75 |
| Bulk Q.ty | 3000 |
| Tube length (± 0.5) | 532 |
| A | 6 |
| B | 21.3 |
| C (± 0.1) | 0.6 |

All dimensions are in mm.

Figure 44. PPAK tape and reel



5 Revision history

Table 16. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 07-Oct-2004 | 1 | Initial release. |
| 24-Nov-2008 | 2 | Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK® packages</i> information. Updated <i>Figure 41: P²PAK tape and reel (suffix "13TR")</i> : – changed component spacing (P) in tape dimensions table from 16 mm to 12 mm. |
| 12-May-2009 | 3 | Removed SO-8 package into the following tables: <i>Table 1, Table 3</i> and <i>Table 4</i> . <i>Figure 2</i> : Removed SO-8 package top view. Removed SO-8 package information in the following sections: <i>Section Note:: Values are generated with $R_L = 0$ W. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.</i> and <i>Section 4: Package and packing information</i> Modified <i>Section 2.1: Absolute maximum ratings</i> and <i>Section 4.1: ECOPACK® packages</i> . |
| 23-Nov-2009 | 4 | Updated features list. Added PENTAWATT in-line package into the document: – Updated <i>Table 1: Device summary</i> – Added <i>Section 4.2.1: PENTAWATT (in-line) mechanical data</i> . |
| 17-Nov-2010 | 5 | Updated following tables: – <i>Table 3: Absolute maximum ratings</i> – <i>Table 4: Thermal data</i> |
| 11-May-2012 | 6 | – Update entire document following ST template. – Update <i>Table 15</i> and <i>Figure 38</i> . |
| 19-Sep-2013 | 7 | Updated Disclaimer. |

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