Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Datasheet describes Mode 0 Operation
- 50 MHz Clock Rate
- Byte Mode and Page Mode Program (1 to 256 Bytes) Operations
- Sector/Block/Page Architecture
  - 256 byte Pages per Sector
  - Eight 4 Kbyte Sectors per Block
  - Four uniform 32 Kbyte Blocks
- Self-timed Sector, Block and Chip Erase
- Product Identification Mode with JEDEC Standard
- Low-voltage Operation
  - 2.7V (V_{CC} = 2.7V to 3.6V)
- Hardware and Software Write Protection
  - Device protection with Write Protect ($\overline{WP}$) Pin
  - Write Enable and Write Disable Instructions
  - Software Write Protection:
    - Upper 1/32, 1/16, 1/8, 1/4, 1/2 or Entire Array
- Flexible Op Codes for Maximum Compatibility
- Self-timed Program Cycle
  - 30 µs/Byte Typical
- Single Cycle Reprogramming (Erase and Program) for Status Register
- High Reliability
  - Endurance: 10,000 Write Cycles Typical
- 8-lead JEDEC 150mil SOIC and 8-lead Ultra Thin Small Array Package (SAP)
- Die Sales: Waffer Form, Tape and Reel, and Bumped Waffers

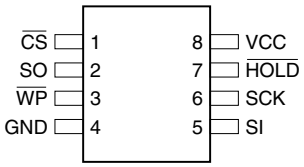
Description

The AT25FS010 provides 1,048,576 bits of serial reprogrammable Flash memory organized as 131,072 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25FS010 is available in a space-saving 8-lead JEDEC SOIC and 8-lead Ultra Thin SAP packages.

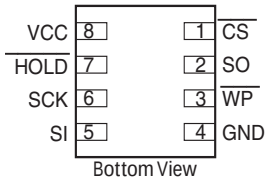
Table 0-1. Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-lead JEDEC SOIC



8-lead SAP



High Speed Small Sectored SPI Flash Memory

1M (131,072 x 8)

AT25FS010

The AT25FS010 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

BLOCK WRITE protection for upper 1/32, 1/16, 1/8, 1/4, 1/2 or the entire memory array is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

1. Absolute Maximum Ratings*

Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +5.0V
Maximum Operating Voltage	4.2V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram

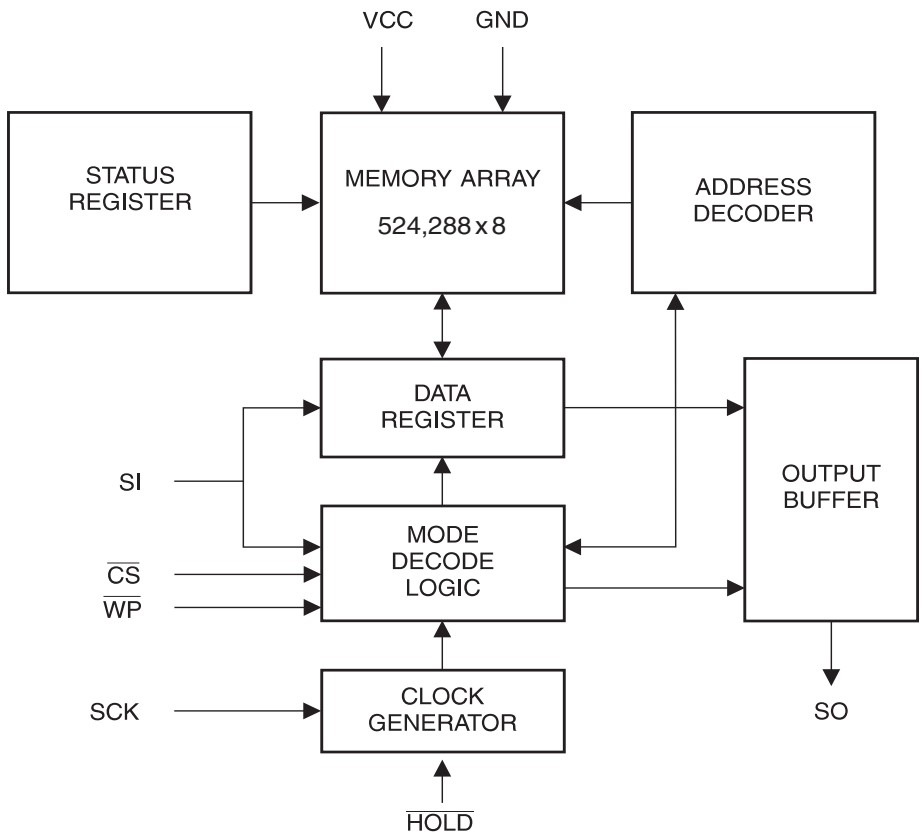


Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +3.6V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics (Preliminary – Subject to Change)

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +2.7V to +3.6V, T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +3.6V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Read			10.0	17.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Write			15.0	45.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			2.0	10.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-3.0		3.0	µA
V_{IL}[1]	Input Low Voltage			-0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics (Preliminary – Subject to Change)

Applicable over recommended operating range from T_A = –40°C to +85°C, V_{CC} = +2.7V to +3.6V
C_L = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency	0		50	MHz
t_{RI}	Input Rise Time			5	ns
t_{FI}	Input Fall Time			5	ns
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			ns
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			ns
t_{SU}	Data In Setup Time	5			ns
t_H	Data In Hold Time	5			ns
t_{HD}	$\overline{Hold}$ Setup Time	5			ns
t_{CD}	$\overline{Hold}$ $\overline{Hold}$ Time	5			ns
t_V	Output Valid			9	ns
t_{HO}	Output Hold Time	0			ns
t_{LZ}	$\overline{Hold}$ to Output Low Z			9	ns
t_{HZ}	$\overline{Hold}$ to Output High Z			9	ns
t_{DIS}	Output Disable Time			9	ns
t_{se}	Sector Erase Time		50	200	ms
t_{be}	Block Erase Time		200	500	ms
t_{ce}	Chip Erase Time		1.6	4	s
t_{SR}	Status Register Write Cycle Time			60	ms
t_{BPC}	Byte Program Cycle Time(1)		30	50	µs
Endurance(2)			10K		Write Cycles(3)

Notes: 1. The programming time for n bytes will be equal to n x t_{BPC}.
2. This parameter is ensured by characterization at 3.0v, 25c only.
3. One write cycle consists of erasing a sector, followed by programming the same sector.

Ordering Information

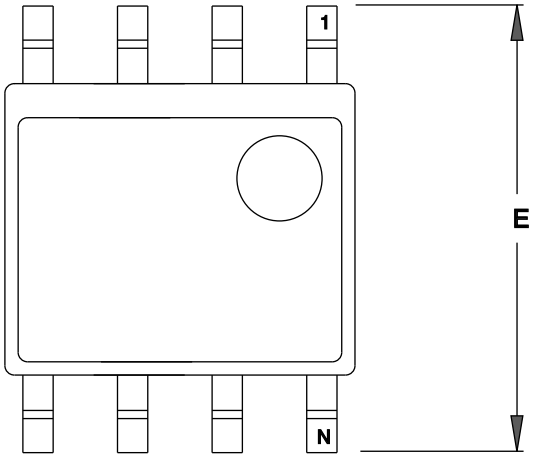
Ordering Code	Package	Operation Range
AT25FS010N-SH27-B[1]	8S1	Lead-Free/Halogen-Free/ NiPdAu Lead Finish Industrial Temperature (–40°C to 85°C)
AT25FS010N-SH27-T[2]	8S1	
AT25FS010Y7-YH27-T[2]	8Y7	

Notes: 1. "-B" designates bulk ordering code.
2. "-T" designates tape and reel ordering code. SOIC=4K per reel and SAP=3K per reel.

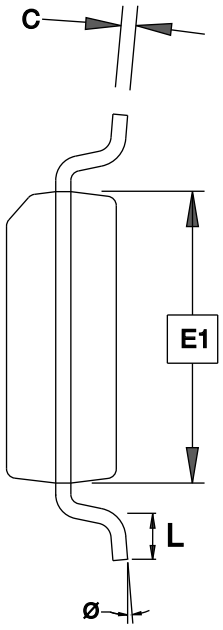
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small outline (JEDEC SOIC)
8Y7	8-lead, 6.00 mm x 4.90 mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP)
Options	
–2.7	Low Voltage (2.7V to 3.6V)

7. Package Information

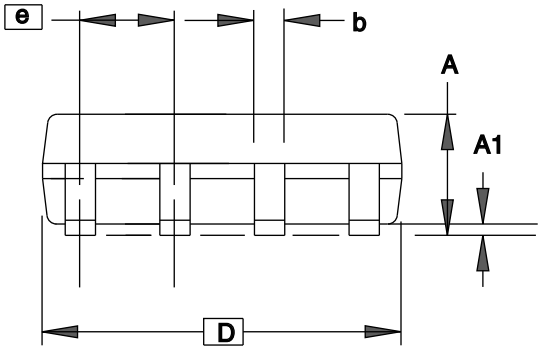
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** C